Multi Channel Power Supply IC for LCD TV/MNT

Features

- **8.6V to 14.7V Input Voltage Range for TV**
- **4.3V to 6V Input Voltage Range for MNT**
- **AVDD Async-Boost Converter: 13.5 ~ 19.8V**
  - ♦ 500/ 750kHz Switching Frequency
  - ♦ 5A Switching Current Limit
  - ♦ Controller by 0.3V Over-Current Protection.
- **External V_{AVDD} Isolation Switch Control**
- **VBK1 Sync Buck Converter: 1.8 ~ 3.35V**
  - ♦ 500/750kHz Switching Frequency
  - ♦ 1.5A Switching Current Limit
- **HAVDD OP**
  - ♦ 1 Channels Programmable HAVDD OP
  - ♦ ±200mA Short Circuit Current
  - ♦ 7-bits DAC resolution
- **VGH Async-Boost Converter/ Charge Pump Regulator: 20 ~ 45V**
  - ♦ 500/ 750kHz Switching Frequency
  - ♦ 1.5A Switching Current Limit
  - ♦ Temperature Compensation: 20V ~ 45V
- **VGL Async-Inverting Converter/ Charge Pump Regulator: -3 ~ -18V**
  - ♦ 500/ 750kHz Switching Frequency
  - ♦ 1.5A Async Inverting Switching Current Limit
  - ♦ Temperature Compensation: -3V ~ -18V
- **VSS1 Negative Regulators: -3V to -16V**
- **14-CH Gamma Buffers**
  - ♦ 14 Channels Rail-to-Rail Programmable Gamma Buffers
  - ♦ 10 Bits Resolution for reach Channel
- **1-CH VCOM1 Buffer**
  - ♦ 1 Channels Programmable VCOM Buffer
  - ♦ 7 Bits Resolution for reach Channel
- **1-CH VCOM2 DAC**
  - ♦ 1 Channels Programmable VCOM DAC
  - ♦ 7 Bits Resolution for reach Channel
- **Integrated MTP Non-Volatile Memory**
- **Programmable Sequence Timing**
- **Over-Temperature Protection**
- **I^2C Compatible Interface for Register Control**
- **Available in 6.5mmX4.5mm 46-pin TQFN Package**

General Description

The G2732P is a programmable multi-functional power solution with integrated gamma buffers, VCOM1 buffer for TFT-LCD. It contains one boost converter/ controller (AVDD), one ISO MOSFET controller for AVDD power on sequence, one buck converter (VBK1), one boost converter/ positive charge pump regulator (VGH) with the temperature compensation, one inverting converter/ negative charge pump regulator (VGL2) with the temperature compensation, one negative regulators (VSS1), 14-CH gamma buffers, 1-CH VCOM1 buffer, 1-CH VCOM2 DAC. All channel output level and sequence can be programmable by I2C interface and integrated Multiple-Time Programmable (MTP) non-volatile memory.

With its high current capabilities, the G2732P is ideal for large screen LCD TV/MNT panel application with widely supply voltage range and also integrated complete protection functions including, OVP, UVP, OCP and OTP. The G2732P available in a TQFN6.5x4.5-46 pin package.

Applications

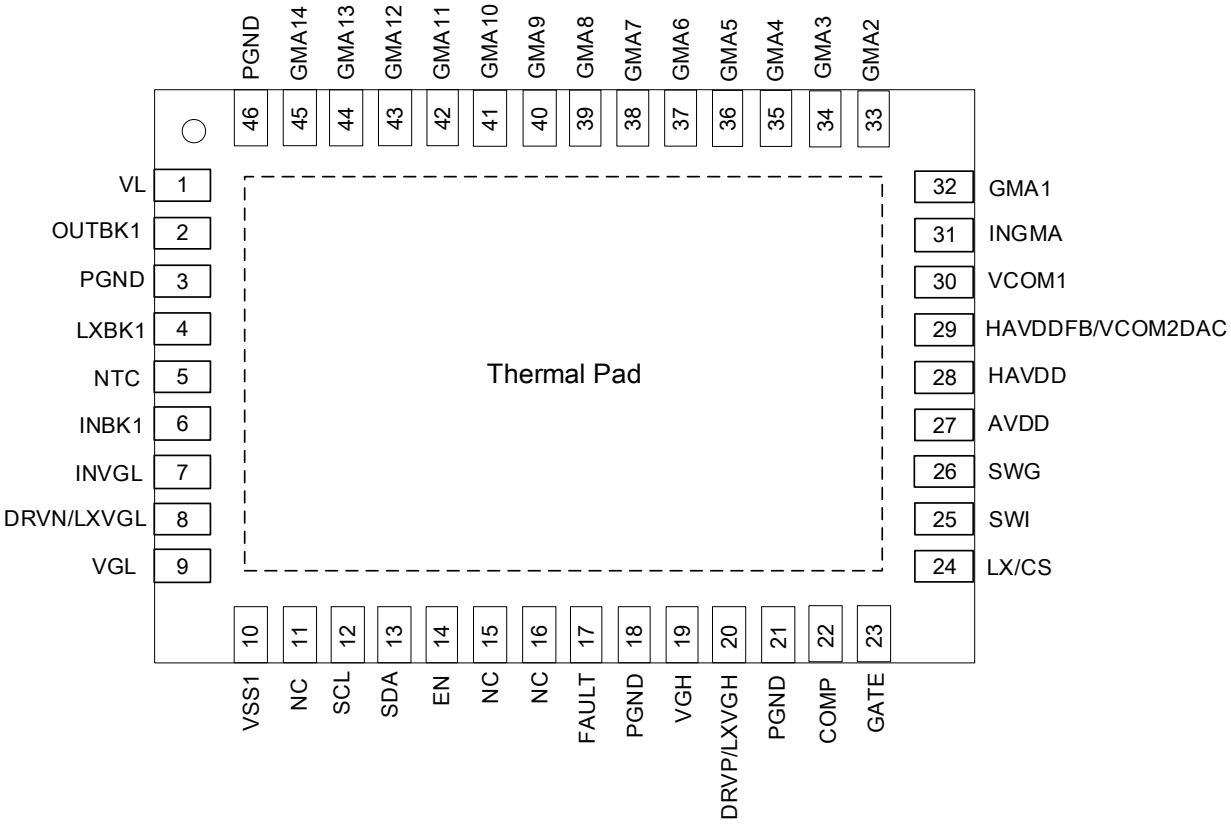
- **TFT LCD Monitor Panel**
- **TFT LCD TV Panel**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2732PK81D-K	2732P	-40°C~ +85°C	TQFN6.5X4.5-46

Note: K8: TQFN6.5X4.5-46
1: Bonding Code
D: Tape & Reel
Green : Lead Free / Halogen Free.

Pin Configuration



G2732P TQFN6.5X4.5-46

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

INBK1, INVGL, to PGND . . . . . -0.3V to 16.5V
SWI, SWG, AVDD to PGND . . . . . -0.3V to 23V
HAVDD, HAVDDFB/VCOM2DAC to PGND . . . . . -0.3V to 23V
LX/CS to PGND . . . . . -0.3V to 23V
LX/CS to SWI . . . . . -0.3V to 23V
SWI to AVDD . . . . . -0.3V to 23V
EN to PGND . . . . . -0.3V to INBK1-0.3V
VL to PGND . . . . . -0.3V to 6V
COMP, NTC, SDA, SCL to PGND. . . . . -0.3V to 6V
LS_SDA, LS_SCL, FAULT to PGND. . -0.3V to 6V
OUTBK1 to PGND . . . . . -0.3V to 6V
GATE to PGND . . . . . -0.3V to 6V
LXBK1 to PGND . . . . . -0.3V to INBK1+0.3V
DRVP/LXVGH, VGH to PGND . . . . . -0.3V to 50V
DRVN/LXVGL, VGL to PGND . . . . . -20V to 0.3V
DRVN/LXVGL to INVGL . . . . . .-40V to 0.3V
VSS1 to PGND . . . . . -20V to 0.3V
VGH to VGL, VSS1 . . . . . -0.3V to 60V
VGL to VSS1 . . . . . -20V to 0.3V
INGMA to GND . . . . . -0.3V to 23V
VCOM1 to PGND . . . . . -0.3V to INGMA+0.3V
GMA1~14 to PGND . . . . . -0.3V to INGMA+0.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN6.5x4.5-46 . . . . . 35°C/W
Thermal Resistance Junction to Case,(θ_{JC})
TQFN6.5x4.5-46. . . . . 7°C/W
Continuous Power Dissipation (T_A = +25°C)
TQFN6.5x4.5-46. . . . . 3.57W
Operating Temperature . . . . . -40°C to 85°C
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . .-65°C to 150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
Electrostatic Discharge, V_{ESD}
Human Body Mode (HBM) 2000V
Machine Mode (MM) 200V

Electrical Characteristics

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Input Voltage Range	V_{IN}	Register address="46h", bit7=0	8.6	---	14.7	V
		Register address="46h", bit7=1	4.3	---	6.0	V
Quiescent Current into V_{INBK1}	$I_{QVINBK1}$	No switching	---	3.5	---	mA
Quiescent Current into V_{INVGL}	$I_{QVINVGL}$	No switching	---	0.15	---	mA
Quiescent Current into V_{INGMA}	$I_{QVINGMA}$	No switching	---	8	---	mA
VIN Under-voltage Lockout Threshold Register address="46h", bit7=0	$V_{UVLOVIN}$	V_{IN} rising	---	8.3	---	V
		Hysteresis	---	800	---	mV
VIN Under-voltage Lockout Threshold Register address="46h", bit7=1	$V_{UVLOVIN}$	V_{IN} rising	---	4.2	---	V
		Hysteresis	---	400	---	mV
VL Output Voltage	V_L	VIN=8.6V~14.7V	4.9	5.0	5.1	V
Thermal Shutdown Protection		Rising	---	150	---	°C
LOGIC						
SDA/SCL/EN Input Level	V_{IH}		1.6	---	---	V
	V_{IL}		---	---	0.6	V
SDA/SCL Input Leakage Current	I_{IH}, I_{IL}	V_I=0V or 3.3V	-1	0.01	1	µA
EN pull down resistor	R_{PD}		320	400	480	kΩ
Input Capacitance			---	5	---	pF
SDA Output Low Voltage	V_{OL}	I_{SINK}=6mA	0.3	---	---	V
ASYNC. BOOST CONVERTER (AVDD)						
AVDD Programmable Output Voltage Range	V_{AVDD}	Register address="46h", bit7=0	13.5	---	19.8	V
		Register address="46h", bit7=1	11	---	17.3	V
SWO Output Accuracy		No load, Default output	-1	---	1	%
N-MOSFET On Resistance	$R_{DS(ON)}$	$I_{LX/CS}$=500mA	---	100	----	mΩ
Transconductance	GM		---	200	---	uA/V
Current-Sense Transresistance	R_{CS}		---	0.25	---	Ω
N-MOSFET Switch Current Limit	I_{LIM}	AVDD OCP	5	---	---	A
Soft-Start Period	SS_{AVDD}	Programmable Soft-Start Time	---	10	---	ms

Electrical Characteristics

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch Leakage Current	I_{LEAK}	$V_{LX/CS}$=19.8V	---	1	10	μA
SWI Over Voltage Protection	V_{OVP}	V_{SWI} Rising, hysteresis = 1V	---	21.8	---	V
AVDD Line Regulation		8.6V≦VIN≦14.7V, I_{AVDD}=1mA	---	0.04	---	%/V
AVDD Load Regulation		1mA≦I_{AVDD}≦1.5A	-1	---	1	%
AVDD UVP Fault Trip Level		V_{AVDD} Falling	---	85	---	%
UVP fault timer duration			---	50	---	ms
SWO Short Circuit Level	V_{SC}	V_{AVDD} Falling	---	20	---	%
Operating Frequency	F_{OSC}	Register address=”29h”, bit7=1	---	500	---	kHz
		Register address=”29h”, bit7=0	---	750	---	kHz
Maximum Duty Cycle			---	90	---	%
Gate Output Hi-Level	V_{GOH}		---	SWI	---	V
Gate Output Low-Level	V_{GOL}		---	SWI-6	---	V
Gate pull-high resistor	R_{AVDD}		---	10	---	kΩ
Gate Sink Current	I_{G_SINK}		---	10	---	μA
Power Off Discharge Resistance	R_{SWO_DCHG}		---	4.7	---	kΩ
External N-MOSFET Gate Driver (Gate of AVDD)						
Gate High Voltage	D_{Gate_OH}		4.5	5	5.5	V
Gate Low Voltage	D_{Gate_OL}		0	---	0.3	V
External NMOS Switch Current Limit	V_{CS_OCP}	R_{CS}=50mΩ	---	0.3	---	V
Gate to VL High-Side On Resistance	$R_{DS\ ON\_GH}$		---	5	---	Ω
Gate to GND Low-Side On Resistance	$R_{DS\ ON\_GL}$		---	5	---	Ω
ASYNC BOOST CONVERTER (VGH)						
Adjustable Normal Temperature Output Voltage Range	V_{GH_NT}	Register address=”03h”, 5bits/26 steps	20	---	45	V
Adjustable Low Temperature Output Voltage Range	V_{GH_LT}	Register address=”04h”, 5bits/26 steps	20	---	45	V
Output voltage tolerance			-3	---	3	%
Operating Frequency	F_{OSC}	Register address=”29h”, bit7=1	---	500	---	kHz
		Register address=”29h”, bit7=0	---	750	---	kHz
Low-Side NMOS Switch on Resistance	$R_{DS(ON)}$		---	0.7	---	Ω
NMOS Switch Current Limit	I_{LIM}		1.5	---	---	A
NMOS Switch Leakage Current	I_{LEAK}	V_{LXVGH}=45V	---	1	---	μA
Line Regulation		V_{AVDD} = 8.6 to 14.7V, I_{GH} = 0.1A	---	0.1	---	%/V
Load Regulation		I_{GH}= 1mA to 0.1A	---	0.3	---	%/A
Soft-Start Time	t_{SS}		---	3	---	ms
Output OVP Fault-Trip Level		V_{GH} rising, hysteresis: 3V	---	48.5	---	V
Output UVP Fault-Trip Level		V_{GH} falling	---	80	---	%
UVP fault timer duration			---	50	---	ms
Output SCP Fault-Trip Level		V_{GH} falling	---	20	---	%
Power Off Discharge Resistance	R_{DIS}		---	30	---	kΩ

Electrical Characteristics

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VGH CHARGE PUMP REGULATOR (VGH)						
Adjustable Normal Temperature Output Voltage Range	V_{GH_NT}	Register address="03h", 5bits/26 steps	20	---	45	V
Adjustable Low Temperature Output Voltage Range	V_{GH_LT}	Register address="04h", 5bits/26 steps	20	---	45	V
Output voltage tolerance			-3	---	3	%
DRVP Leakage Current		V_{DRVP} =40V	---	1	10	µA
DRVP Sink Current			---	5	---	mA
DRVP Short Circuit Current	$I_{DRVP,SC}$	V_{GH}<V_{GH}*20%	---	400	---	µA
Line Regulation		V_{AVDD} = 8.6 to 14.7V, I_{GH} = 0.1A	---	0.1	---	%/V
Load Regulation		V_{DRVP}=10V, I_{DRVP}= 50µA to 1mA	---	0.4	---	%
Soft-Start Time	t_{SS}	Register address="2Dh", bit0=0	---	3	---	ms
Soft-Start Time	t_{SS}	Register address="2Dh", bit0=1	---	6	---	ms
Output OVP Fault-Trip Level		V_{GH} rising, hysteresis: 3V	---	48.5	---	V
Output UVP Fault-Trip Level		V_{GH} falling	---	80	---	%
UVP fault timer duration			---	50	---	ms
Output SCP Fault-Trip Level		V_{GH} falling	---	20	---	%
Power Off Discharge Resistance	R_{DIS}		---	30	---	kΩ
VGL INVERTING CONVERTER (VGL)						
Adjustable Normal Temperature Output Voltage Range	V_{GL_NT}	Register address="05h", 5bits/31 steps	-18	---	-3	V
Adjustable Low/High Temperature Output Voltage Range	$V_{GL\_LT/HT}$	Register address="06h", 5bits/31 steps	-18	---	-3	V
Output Voltage Tolerance		No load, Default output	-3	---	3	%
Operating Frequency	F_{OSC}	Register address="29h", bit7=1	---	500	---	kHz
Operating Frequency	F_{OSC}	Register address="29h", bit7=0	---	750	---	kHz
Maximum Duty Cycle			80	90	---	%
PMOS Switch On-Resistance	$R_{DS(ON)}$	I_{VGL_SW} = 100mA	---	0.65	---	Ω
Minimum On Time			---	100	---	ns
PMOS Switch Current Limit	I_{LIM}		1.5	---	---	A
PMOS Switch Leakage Current	I_{LEAK}	V_{GL_SW}=VIN or V_{GL}	---	5	---	µA
Line Regulation		V_{IN} = 8.6 to 14.7V, I_{GL} = 0.1A	---	0.1	---	%/V
Load Regulation		I_{GL} = 200mA to 500mA	---	0.3	---	%/A
Soft-Start Time	t_{SS}		---	3	---	ms
Output OVP Fault-Trip Level		V_{GL} falling, hysteresis: 105%	---	120	---	%
Output UVP Fault-Trip Level		V_{GL} rising	---	80	---	%
UVP fault timer duration			---	50	---	ms
Output SCP Fault-Trip Level		V_{GL} rising	---	20	---	%
Power Off Discharge Resistance	R_{DIS}		---	12	---	kΩ

Electrical Characteristics (continued)

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VGL CHARGE PUMP REGULATOR (VGL)						
Adjustable Normal Temperature Output Voltage Range	V_{GL_NT}	Register address="05h", 5bits/31 steps	-18	---	-3	V
Adjustable Low/High Temperature Output Voltage Range	$V_{GL\_LT/HT}$	Register address="06h", 5bits/31 steps	-18	---	-3	V
Output Voltage Tolerance		No load, Default output	-3	---	3	%
DRVN Leakage Current		V_{DRVN} = -15V	-1	1	10	µA
DRVN Source Current			---	10	---	mA
DRVN Short Circuit Current	$I_{DRVN,SC}$	V_{GL}>V_{GL}*20%	---	400	---	µA
Line Regulation		V_{IN} = 8.6 to 14.7V, I_{GL} = 0.1A	---	0.1	---	%/V
Load Regulation		V_{DRVN}=10V, I_{DRVN}=50µA to 1mA	---	0.7	---	%
Soft-Start Time	t_{SS}		---	3	---	ms
Output OVP Fault-Trip Level		V_{GL} falling, hysteresis: 0.5V	---	120	---	%
Output UVP Fault-Trip Level		V_{GL} rising	---	80	---	%
UVP fault timer duration			---	50	---	ms
Output SCP Fault-Trip Level		V_{GL} rising	---	20	---	%
Power Off Discharge Resistance	R_{DIS}		---	10	---	kΩ
VSS1 NEGATIVE REGULATOR (VSS1)						
Adjustable Output Voltage Range	V_{SS1}	Register address="07h",5bits/27 steps	-16	---	-3	V
Output Voltage Tolerance		No load, Default output	-3	---	3	%
Current Limit	I_{LIM}		---	100	---	mA
Soft-Start Time	t_{SS}		---	3	---	ms
Output UVP Fault-Trip Level		V_{SS1} falling	---	80	---	%
UVP fault timer duration			---	50	---	ms
Integral Nonlinearity	INL	No load	-1	---	1	LSB
Differential Nonlinearity	DNL	No load	-1	---	1	LSB
Load Regulation		I_{SS1} = -50mA to 50mA	---	±0.5	---	mV/mA
Power Off Discharge Resistance	R_{DIS}		---	1.2	---	kΩ
THERMAL COMPENSATION (VGH&VGL&VCOM1)						
VGH & VGL lower bound Voltage of VTC1	V_{TC1}	Register address="2Eh", 4bits/16 steps	0.4	---	3.4	V
VGH & VGL upper bound Voltage of VTC2	V_{TC2}	Register address="2Eh", 4bits/16 steps	0.4	---	3.4	V
VCOM lower bound Voltage of VTC1	V_{TC1}	Register address="2Fh", 4bits/16 steps	0.4	---	3.4	V
VCOM upper bound Voltage of VTC2	V_{TC2}	Register address="2Fh", 4bits/16 steps	0.4	---	3.4	V

Electrical Characteristics (continued)

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HAVDD OPAMP (VHAVDD)						
HAVDD voltage resolution			---	7	---	bits
Integral Nonlinearity	INL	No load	-4	---	+4	LSB
Differential Nonlinearity	DNL	No load	-1	---	+1	LSB
Output voltage swing high	V_{OH}	I_{HAVDD}= +100mA	---	V_{AVDD}-2	---	V
Output voltage swing low	V_{OL}	I_{HAVDD}= -100mA	---	2	---	V
Short-Circuit Current	I_{SC}		---	±200	---	mA
Input common-mode rejection ratio	CMRR	AVDD=15V, F=10kHz, 2V amplitude sin signal	---	80	---	dB
Power supply rejection ratio	PSRR	AVDD sweeps from 8V to 18V	---	60	---	dB
Slew rate	SR		---	45	---	V/µs
-3dB bandwidth	BW		---	20	---	MHz
Output OVP fault-trip level		V_{HAVDD} rising	---	120	---	%
OVP fault timer duration			---	50	---	ms
Output UVP fault-trip level		V_{HAVDD} falling	---	80	---	%
UVP fault timer duration			---	50	---	ms
Power Off Discharge Resistance	R_{DIS}		---	10	---	kΩ
SYNC BUCK CONVERTER (VBK1)						
Programmable Output Voltage Range	V_{BK1}	Register address="01h", 5bits/32 steps	1.8	---	3.35	V
Output Voltage Tolerance		No load, Default output	-2	---	2	%
Operating Frequency	F_{OSC}	Register address="29h", bit7=1	---	500	---	kHz
Operating Frequency	F_{OSC}	Register address="29h", bit7=0	---	750	---	kHz
Maximum Duty Cycle			---	90	---	%
High-Side PMOS Switch On Resistance	$R_{DS(ON)\_HS}$	I_{LXBK1}=500mA	---	400	---	mΩ
Low-Side NMOS Switch On Resistance	$R_{DS(ON)\_LS}$	I_{LXBK1}= -500mA	---	200	---	mΩ
High-Side PMOS Switch Current Limit	I_{LIM}		1.5	---	---	A
High-Side Switch Leakage Current	I_{LEAK_HS}	V_{LXBK1}=0V	---	1	10	µA
Low-Side Switch Leakage Current	I_{LEAK_LS}	V_{LXBK1_SW}=12V	---	1	10	µA
Line Regulation		V_{IN}=8.6 to 14.7V, I_{BK1}=500mA	---	0.05	---	%/V
Load Regulation		I_{VBK1}=1mA to 2.5A	-1	---	1	%
Soft-Start Time	t_{SS}		---	3	---	ms
Output OVP Fault-Trip Level		V_{VBK1} rising	---	120	---	%
Output UVP Fault-Trip Level		V_{VBK1} falling	---	80	---	%
UVP fault timer duration			---	50	---	ms
Output SCP Fault-Trip Level		V_{VBK1} falling	---	20	---	%
Power Off Discharge Resistance	R_{DIS}		---	1	---	kΩ

Electrical Characteristics (continued)

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GAMMA BUFFERS (GMA1 to GMA14)						
Supply Range	V_{SWO_GMA}		13.5	---	19.8	V
Gamma Voltage Resolution		GMA1 to 14; 10bits/1024 steps	---	V_{AVDD}/ 1024	---	V
Integral Nonlinearity	INL	No load	-4	---	+4	LSB
Differential Nonlinearity	DNL	No load	-1	---	+1	LSB
Output Voltage Range	$V_{GMA1\ to\ 14}$	$I_{GMA1\ to\ 14}$= sinking or sourcing 5mA	PGND +0.2	---	V_{AVDD}-0.2	V
Output Current	I_{OUT}	$V_{GMA1\ to\ 14}$ drop 0.5V	---	±50	---	mA
Short-Circuit Current	I_{SC}	$V_{GMA1\ to\ 14}$ to V_{SWO_GMA} or PGND	---	±100	---	mA
Program to Output Delay	t_{D_GMA}	From ACK falling edge to programming gamma change 50% voltage at output	---	15	---	µs
Load Regulation		$I_{GMA1\ to\ 14}$ = -12mA to 12mA	---	±0.5 +Rd	---	mV/mA
VCOM1 BUFFERS & VCOM2 DAC (VCOM1 & VCOM2)						
Supply Range	V_{SWO_GMA}		13.5	---	19.8	V
Adjustable Normal Temperature Output Voltage Range	V_{COM1_NT} /$V_{COM2DAC}$	Register address="08h", 7bits/128 steps Res1=(VCOM_MAX-VCOM_MIN)/127	0*Res1+ VCOM_MIN	---	127*Res1+ VCO_MMIN	V
Adjustable Low Temperature Output Voltage Range	V_{COM1_HT}	Register address="09h", 7bits/128 steps Res1=(VCOM_MAX-VCOM_MIN)/127	0*Res1+ VCOM_MIN	---	127*Res1+ VCOM_MIN	V
Adjustable VCOM_MAX	V_{COM_MAX}	Register address="0Ah", 7bits/128 steps	1*(V_{AVDD}/ 128)	---	128*(V_{AVDD}/ 128)	V
Adjustable VCOM_MIN	V_{COM_MIN}	Register address="0Bh", 7bits/128 steps	0*(V_{AVDD}/ 128)	---	127*(V_{AVDD}/ 128)	V
VCOM1 & VCOM2DAC Voltage Resolution		VCOM1&VCOM2DAC will be clamped between VCOM_MAX and VCOM_MIN	---	V_{AVDD}/ 128	---	V
Integral Nonlinearity	INL	No load	-4	---	+4	LSB
Differential Nonlinearity	DNL	No load	-1	---	+1	LSB
Output Voltage Range	V_{COM1} $V_{COM2DAC}$	VCOM1, VCOM2DAC will be clamped between VCOM_MAX and VCOM_MIN	PGND +0.5	---	V_{AVDD}-0.5	V
Short-Circuit Current	I_{SC}	V_{COM1} to V_{INGMA} or PGND	---	±400	---	mA
Program to Output Delay	t_{D_VCOM1} $t_{D\_VCOM2DAC}$	From ACK falling edge to programming VCOM change 50% voltage at output	---	1	---	µs
Load Regulation		I_{COM1}= -100mA to 100mA	-1	±0.5	1	mV/mA
Power Off Discharge Resistance	VCOM1_ R_{DIS}	Register address="2Ch", 2bits/4 steps	Disable	---	8	kΩ

Electrical Characteristics (continued)

(V_{IN}=12V, V_{AVDD}=16V, V_{BK1}=3.3V, V_{HAVDD}=8V, V_{VGH}=28V, V_{VSS1}=-6V, V_{VGL}=-10V with typical values T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT SIGNAL (FAULT)						
FAULT Pull Up Resistance	R_{FAULT}		---	100	---	kΩ
FAULT High Level Input Voltage	V_{FAULT_HIV}		2	---	---	V
FAULT Low Level Input Voltage	V_{FAULT_LIV}		---	---	1	V
FAULT ON Voltage		I_{IN}=3mA	---	---	0.5	V
I²C TIMING CHARCTERISTICS						
Serial-Clock Frequency	f_{SCL}		1	---	400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1300	---	---	ns
Hold Time (Repeated) START Condition	$t_{HD,STA}$		600	---	---	ns
SCL Pulse-Width Low	t_{LOW}		1300	---	---	ns
SCL Pulse-Width High	t_{HIGH}		600	---	---	ns
Setup Time for a Repeated START Condition	$t_{SU,STA}$		600	---	---	ns
Data Hold Time	$t_{HD,DAT}$		50	---	800	ns
Data Setup Time	$t_{SU,DAT}$		100	---	---	ns
SDA and SCL Receiving Rise Time	t_R	(Note 1)	$20+0.1C_B$	---	300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 1)	$20+0.1C_B$	---	300	ns
SDA Transmitting Fall Time	t_F	(Note 1)	$20+0.1C_B$	---	250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		600	---	---	ns
Bus Capacitance	C_B		---	---	400	pF
Pulse Width of Suppressed Spike	t_{SP}		---	85	---	ns
EEPROM start Up Blanking Time		IC power up initialize (Note 2)	---	30	40	ms
Program EEPROM Blanking Time		(Note 2)	---	45	60	ms
Read EEPROM Blanking Time		(Note 2)	---	1.5	5	ms

Note 1: C_B is in pF.

Note 2: The blanking time is defined as the duration of I²C REG. write to or load from EEPROM.

Note 3: For boost converter application. Output voltage must larger than input voltage, so (AVDD-VIN) must larger 1.5V (AVDD-VIN)>1.5).

Pin Description

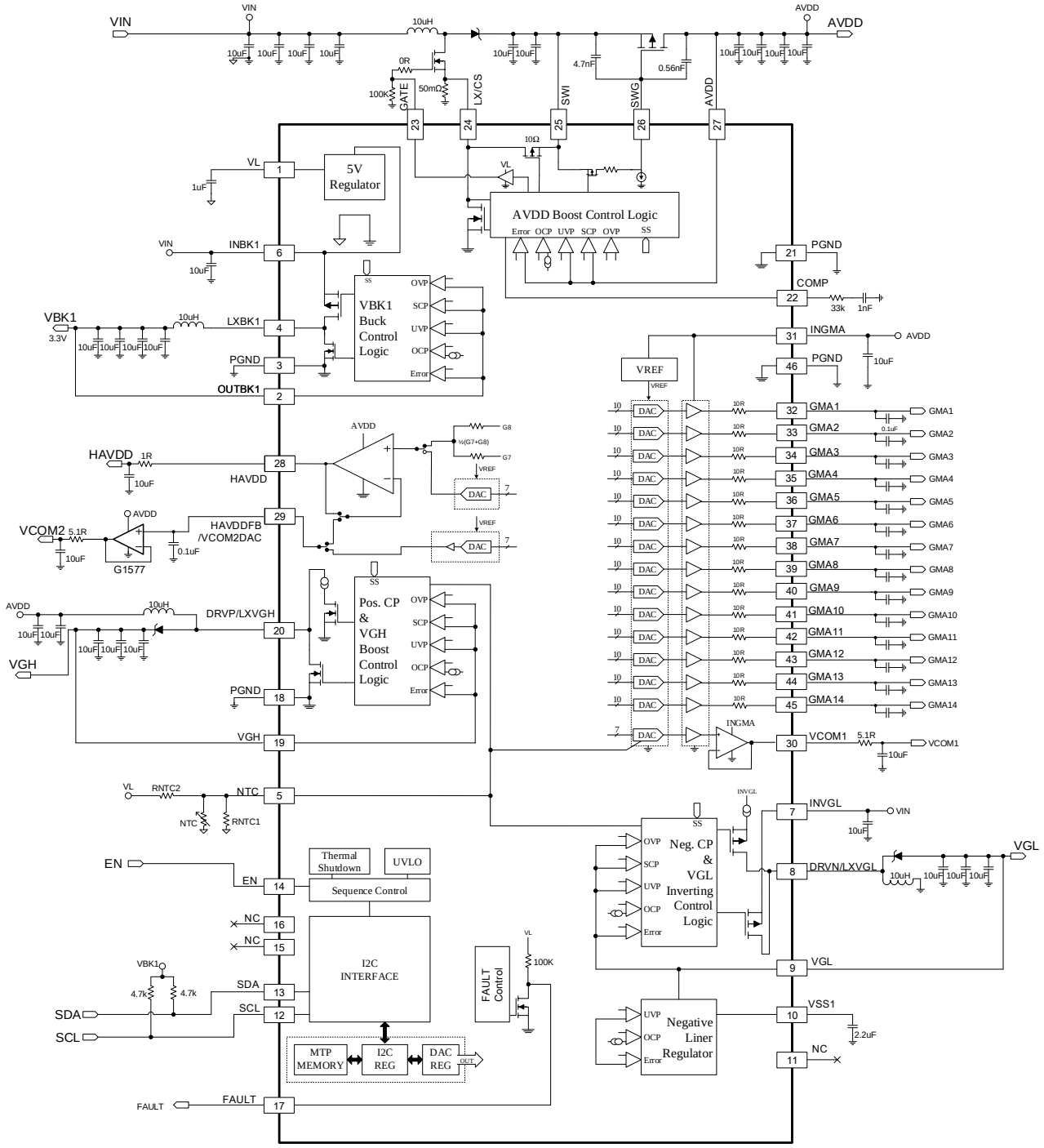
PIN	NAME	I/O	FUNCTION
1	VL	O	5V internal linear regulator output.
2	OUTBK1	I	Feedback voltage input for VBK1 buck converter.
3	PGND	--	Power ground.
4	LXBK1	I/O	Switch node of the VBK1 Buck converter
5	NTC	I	Temperature compensation node, Connect NTC thermistor and resistors to this pin to control the slope of VGH/VGL/VCOM1 voltage for temperature compensation.
6	INBK1	I	Supply voltage input of VBK1 Buck converter.
7	INVGL	I	Supply voltage input of the Inverting converter.
8	DRVN/LXVGL	I/O	DRVN: VGL charge pump mode, for negative linear regulator base drive. LXVGL: VGL inverting mode, for switch node of the inverting converter.
9	VGL	I	VGL charge pump mode, for feedback voltage input for VGL charge pump regulator. VGL inverting mode, for feedback voltage input for VGL inverting converter.
10	VSS1	I	Negative supply voltage of DISCHG1.
11	NC	--	Floating this pin. Do not connect to any other pins or circuit.
12	SCL	I	Clock input pin of the I2C serial interface.
13	SDA	I/O	Data input pin of the I2C serial interface.
14	EN	I/O	@31h, bit7=0, Enable pin of the AVDD, VGH, HAVDD, VCOM1, VCOM2DAC and Gamma. Enable pin must be connect high signal. 400kohm pull down resistor connect from this pin to ground. @31h, bit7=1, XON pin for the shutdown reset function output and open drain voltage detector output.
15	NC	--	Floating this pin, Do not connect to any others pins or circuit.
16	NC	--	Floating this pin, Do not connect to any others pins or circuit.
17	FAULT	I/O	FAULT signal input/output pin. The FAULT pin is open drain output with internal pull up resistor. The output High/Low depended on protection functions. It also can be connected the open drain circuit to control IC operations. (1) Output channel UVP/SCP except VBK1 channel: FAULT_O pin is Low active and all output channel shutdown except VBK1. (2) VBK1 UVP/SCP: FAULT_O pin is Low active and all output channel shutdown) (3) External signal: FAULT_I pin is Low active and all output channel shutdown except VBK1.
18	PGND	--	Power ground.
19	VGH	I	VGH charge pump mode, for feedback voltage input for VGH charge pump regulator. VGH boost mode, for feedback voltage input for VGH boost converter.
20	DRVP/LXVGH	I/O	DRVP: VGH charge pump mode, for positive linear regulator base drive. LXVGH: VGH boost mode, for switch node of the boost converter.
21	PGND	--	Power ground.
22	COMP	I/O	Compensation pin for AVDD Boost converter
23	GATE	I	External N MOSFET gate driver for AVDD external mode.
24	LX/CS	I/O	LX : Switch node of the AVDD Boost converter for AVDD internal mode. CS : External current sense for AVDD external mode.
25	SWI	I	Source input of the AVDD Boost converter external isolation P MOSFET.
26	SWG	I	Gate driver of the AVDD Boost converter external isolation P MOSFET.
27	AVDD	O	Drain output of the AVDD Boost converter external isolation PMOSFET and Feedback voltage input of the AVDD Boost converter

Pin Description (continued)

PIN	NAME	I/O	FUNCTION
28	HAVDD	O	Output of the HAVDD OPAMP.
29	HAVDDFB / VCOM2DAC	I	Negative input of the HAVDD OPAMP. / VCOM2 DAC output.
30	VCOM1	O	VCOM1 operational amplifier output.
31	INGMA	I	Supply voltage input of Gamma buffer and VCOM1 OP.
32	GMA1	O	Gamma DAC analog output 1.
33	GMA2	O	Gamma DAC analog output 2.
34	GMA3	O	Gamma DAC analog output 3.
35	GMA4	O	Gamma DAC analog output 4.
36	GMA5	O	Gamma DAC analog output 5.
37	GMA6	O	Gamma DAC analog output 6.
38	GMA7	O	Gamma DAC analog output 7.
39	GMA8	O	Gamma DAC analog output 8.
40	GMA9	O	Gamma DAC analog output 9.
41	GMA10	O	Gamma DAC analog output 10.
42	GMA11	O	Gamma DAC analog output 11.
43	GMA12	O	Gamma DAC analog output 12.
44	GMA13	O	Gamma DAC analog output 13.
45	GMA14	O	Gamma DAC analog output 14.
46	PGND	--	Power ground.
47	EP	--	Exposed pad. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

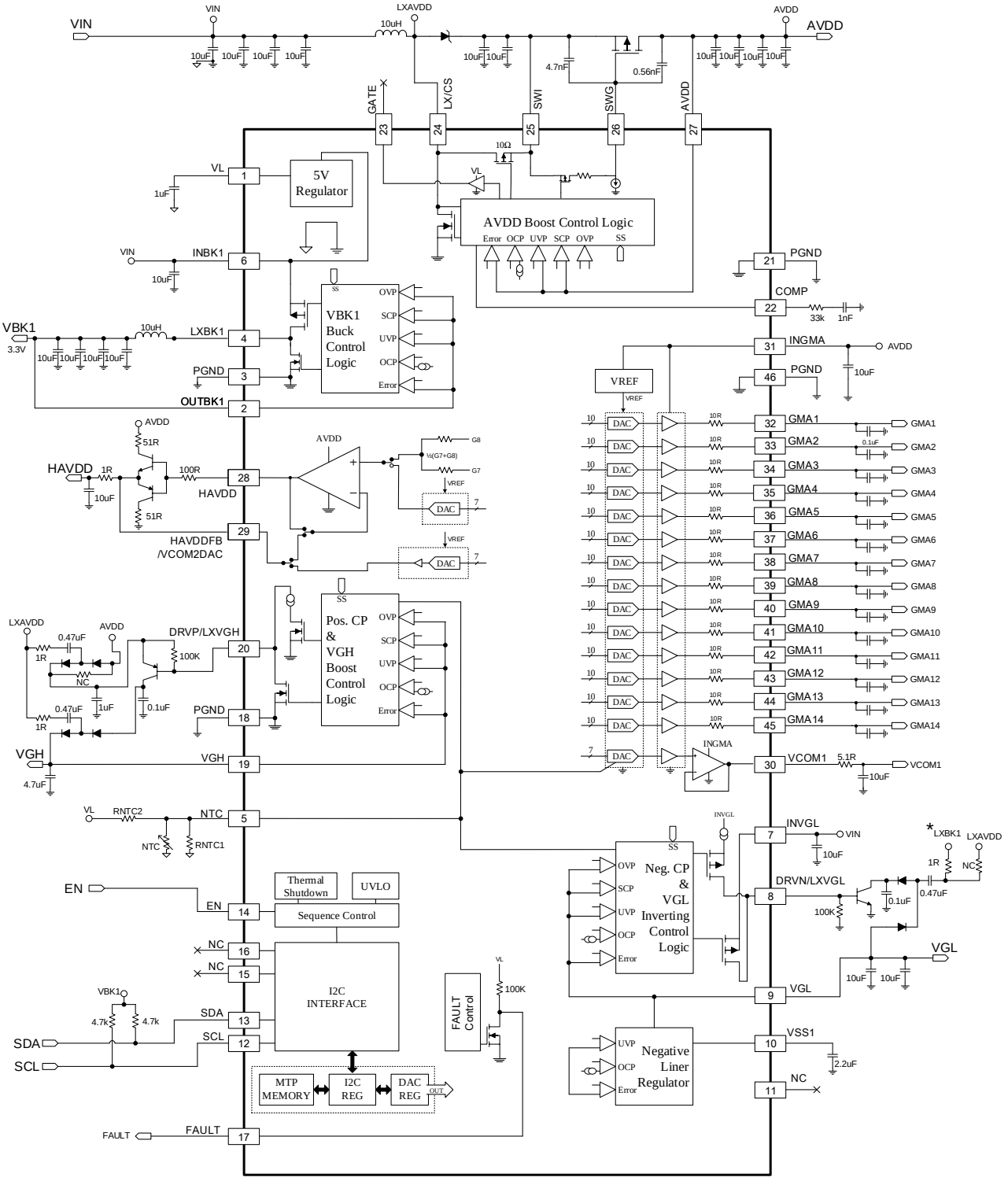
Application Circuit 1

AVDD external mode, VGH boost type, VGL inverting type, HAVDD Internal FB, VCOM2 Enable



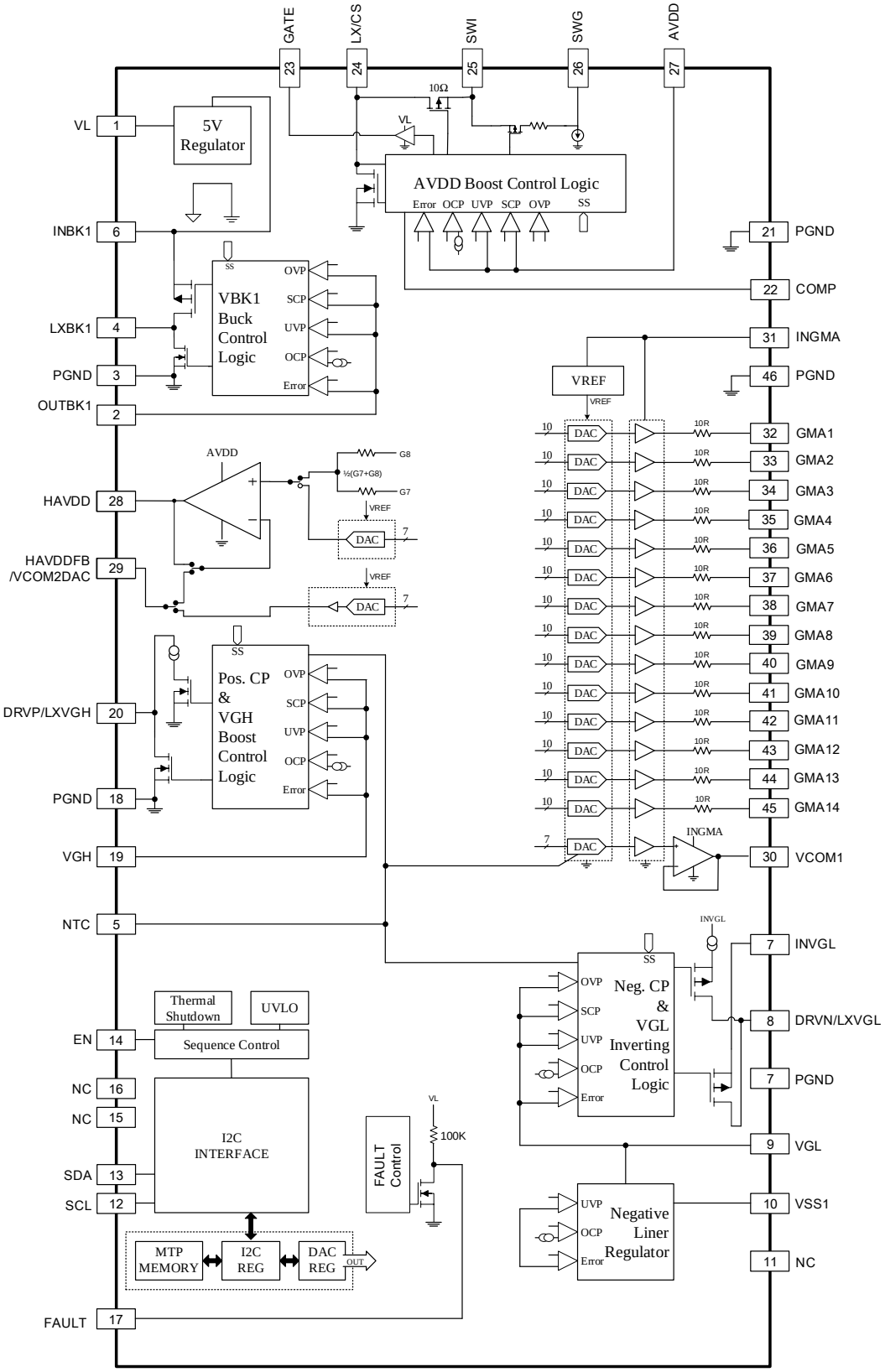
Application Circuit 2

AVDD internal mode, VGH charge pump type and VGL charge pump type HAVDD External FB, VCOM2 Disable



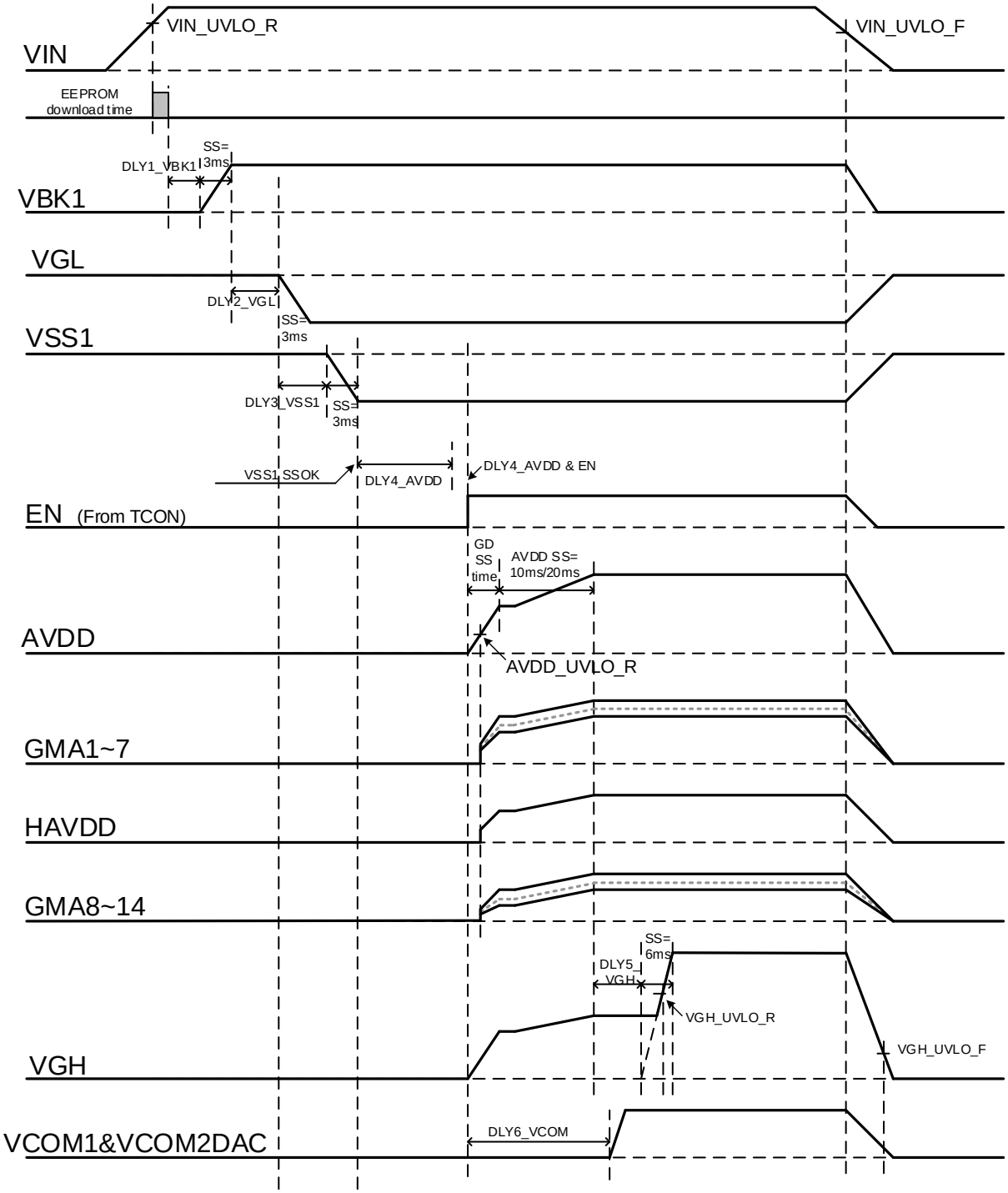
* VGL Charge pump type use LXBK1 only for TV Mode [@[46h] bit7=0]

Block Diagram



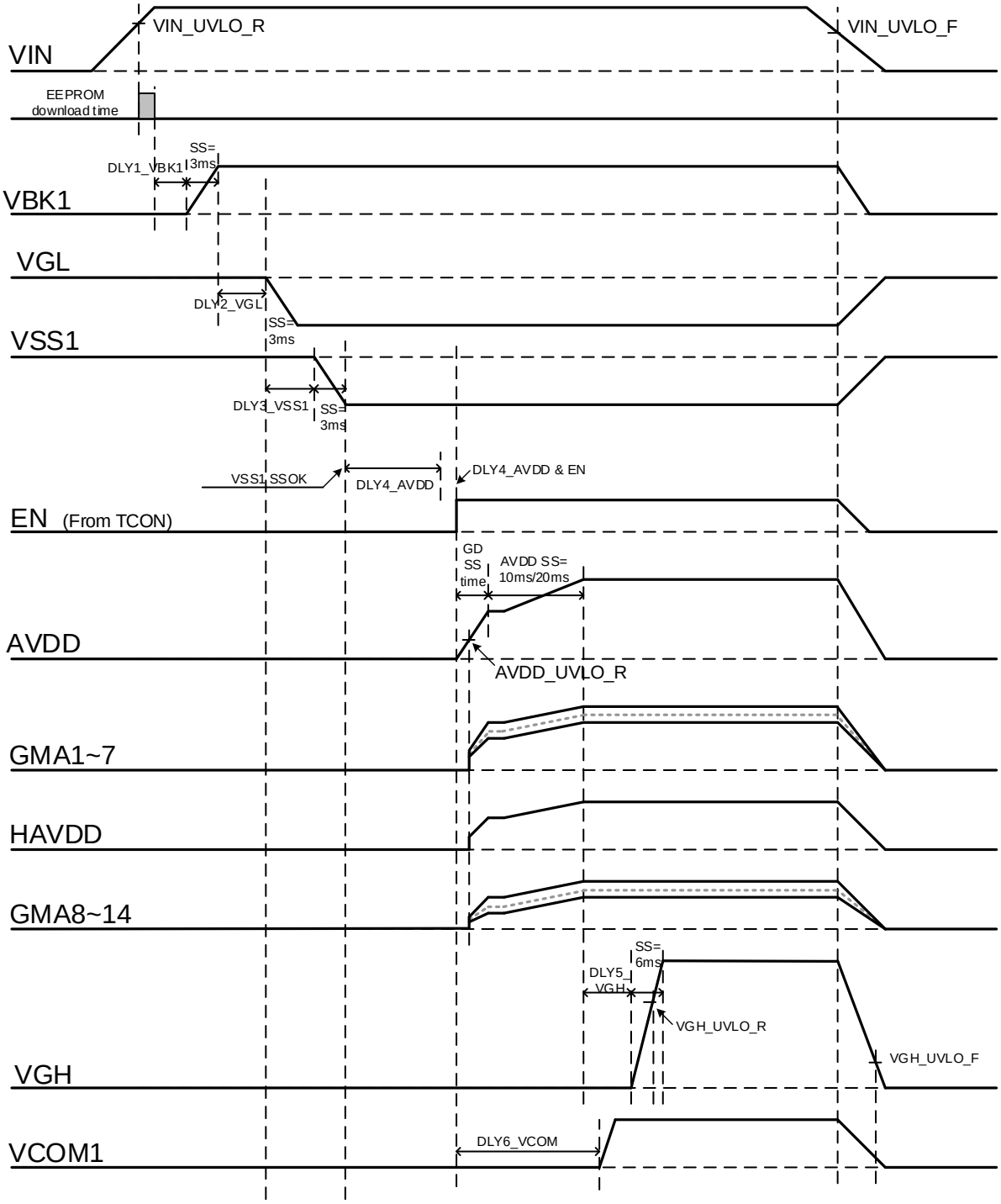
Timing Diagram 1

AVDD external mode, VGH boost type, VGL inverting type and VCOM2



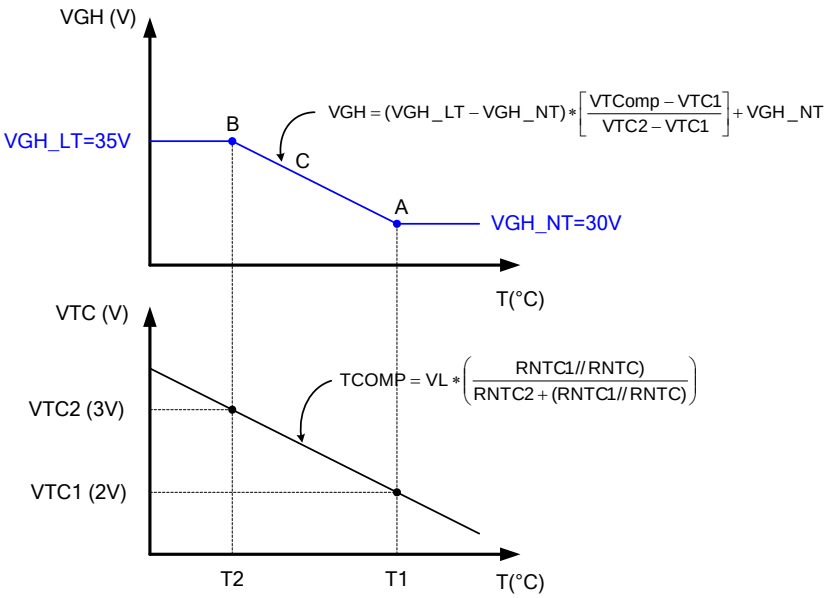
Timing Diagram 2

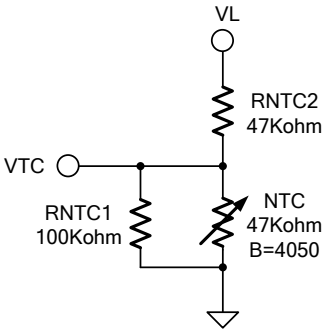
AVDD internal mode, VGH charge pump type and VGL charge pump type



VGH/ VGL/ VCOM1 Temperature Compensation

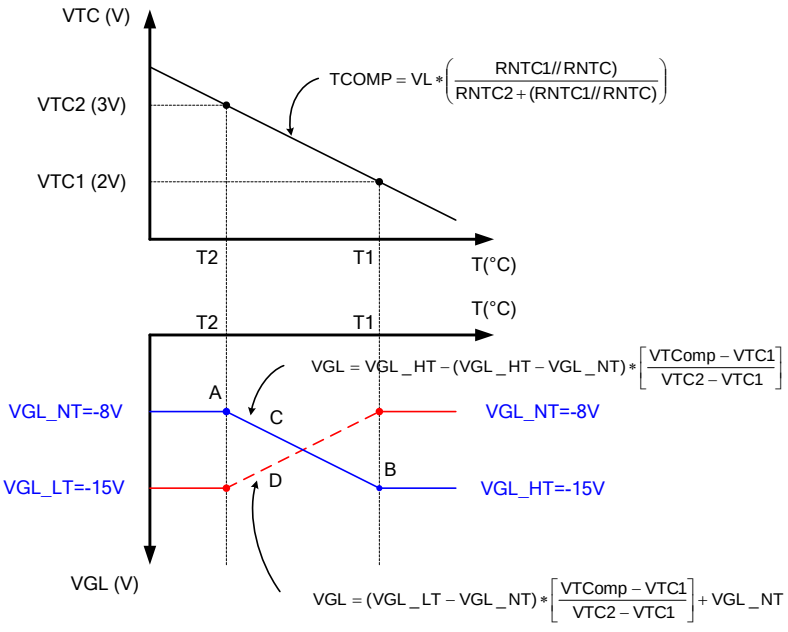
VGH temperature compensation curve

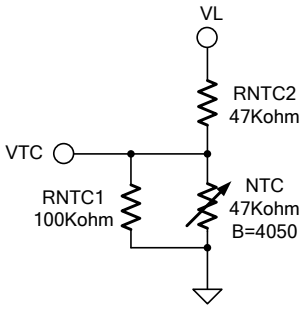




C Curve is temperature compensation

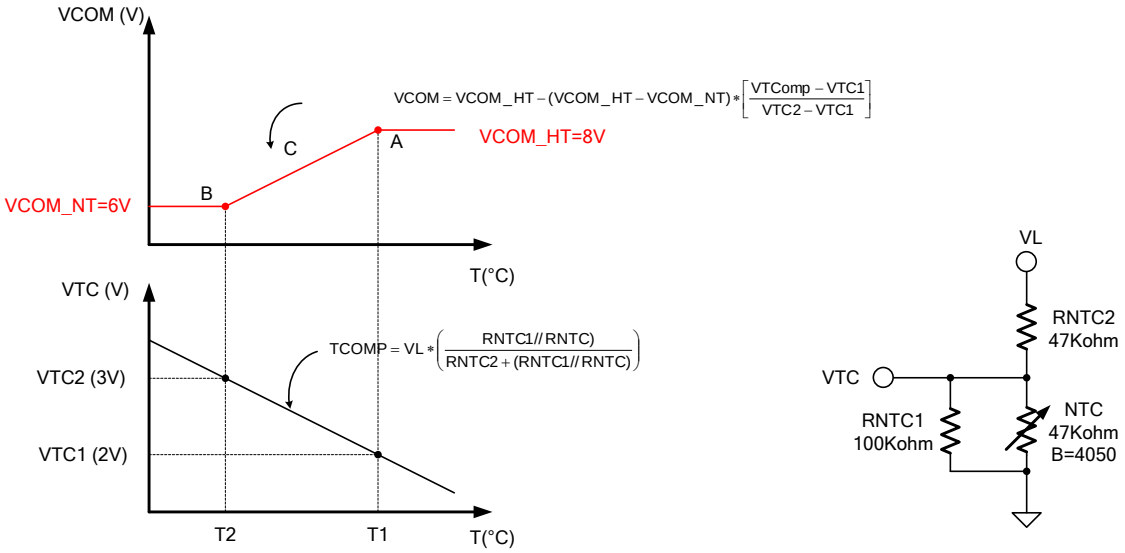
VGL temperature compensation curve





C Curve is negative temperature compensation
D Curve is positive temperature compensation

VCOM1 temperature compensation curve



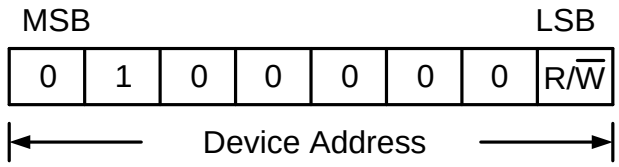
C Curve is temperature compensation

Memory Description

A non-volatile EEPROM containing the initial values of the DACs and a volatile memory containing the DACs settings is implemented in the G2732P. DAC Register and EEPROM Writes and reads can be made directly to the DAC register to control and monitor the position without any nonvolatile memory changes. The nonvolatile memory stores the power on value. When power on, the contents of the EEPROM are transferred to the DAC register. To write to the memory, first program all data registers (00h to 31h & 45h-46h). Then, set the write data bit once all desired data are addressed after power on. To write a new value to the memory, set a new power on position and load the same value into the DAC register. When write address FFh and data register 80h, it will write all DAC register data into EEPROM. Reading from the memory will not change the DAC register if its contents are different.

I²C Command

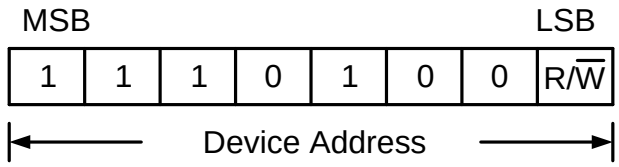
Slave Address



Read Address	Write Address
01000001 (41h)	01000000 (40h)

Note: Device Address 40h, 41h for all PMIC control

Slave Address



Read Address	Write Address
11101001(E9h)	11101000(E8h)

Note: Device Address E8h, E9h only for VCOM1_NT control

I²C Serial-Interface

The G2732P communicates through an industry standard 2-wire I²C serial-interface to receive data in slave mode. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. A master device, usually a microcontroller or a digital signal processor, controls the bus. The I²C serial-interface timing is shown in Figure 1.

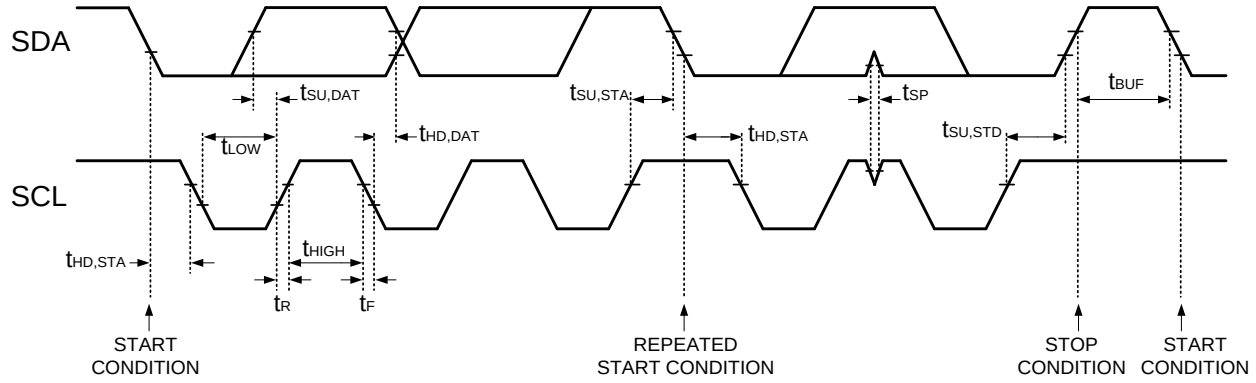
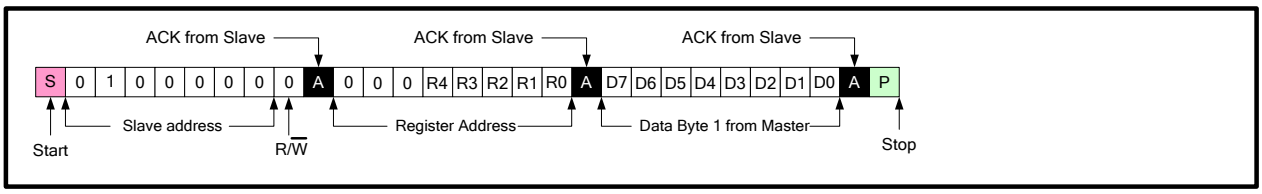


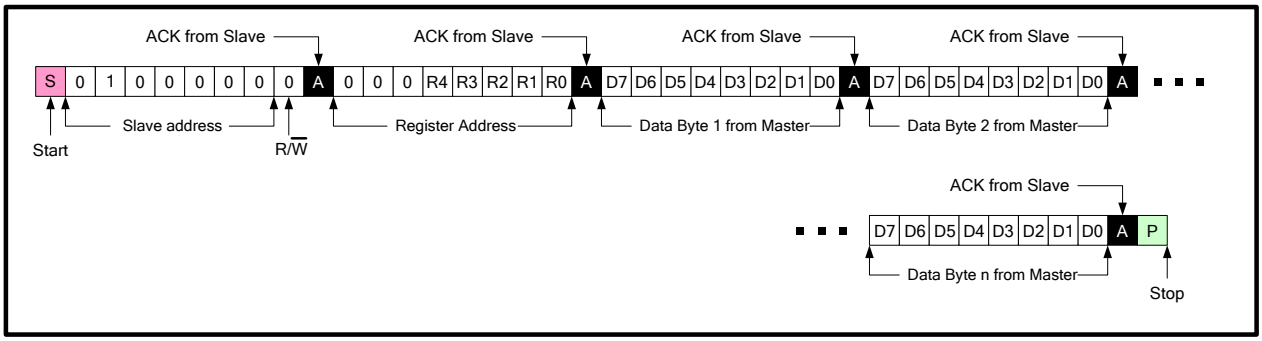
Figure 1. I²C Serial-Interface timing diagram

I2C Commend
Device address (40h/41h)

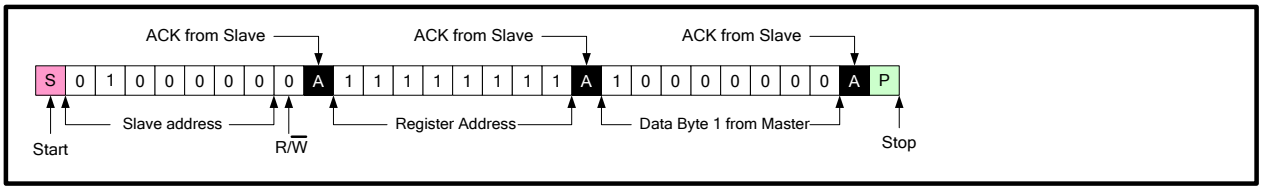
1. Write single byte of data to DAC register


ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 0 0 0 R4 R3 R2 R1 R0 A D7 D6 D5 D4 D3 D2 D1 D0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

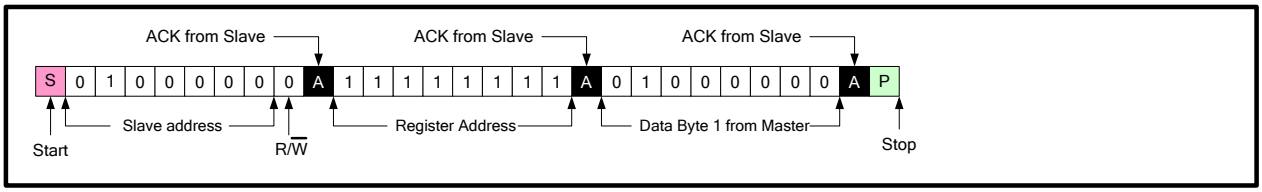
2. Write multiple bytes of data to DAC registers


ACK from Slave
ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 0 0 0 R4 R3 R2 R1 R0 A D7 D6 D5 D4 D3 D2 D1 D0 A D7 D6 D5 D4 D3 D2 D1 D0 A
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Data Byte 2 from Master
ACK from Slave
D7 D6 D5 D4 D3 D2 D1 D0 A P
Data Byte n from Master
Stop

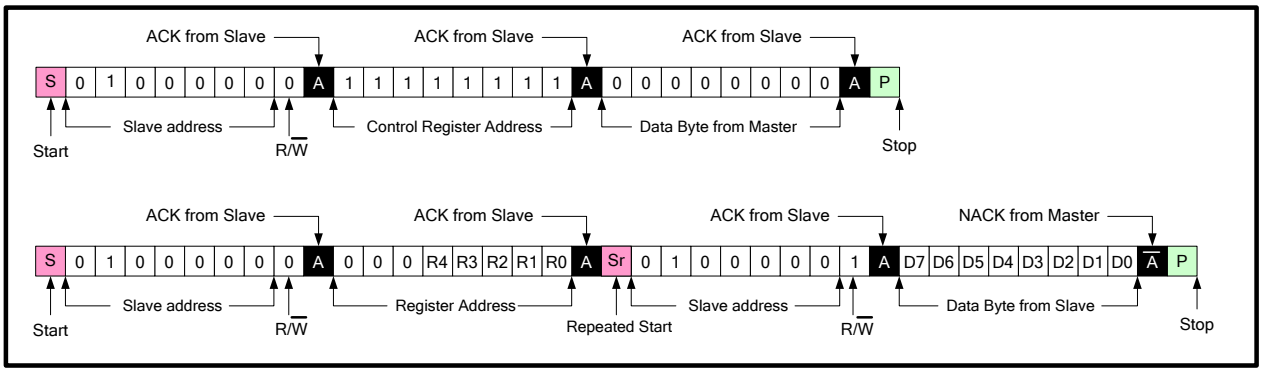
3. Write all registers into EEPROM


ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 1 1 1 1 1 1 1 1 A 1 0 0 0 0 0 0 0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

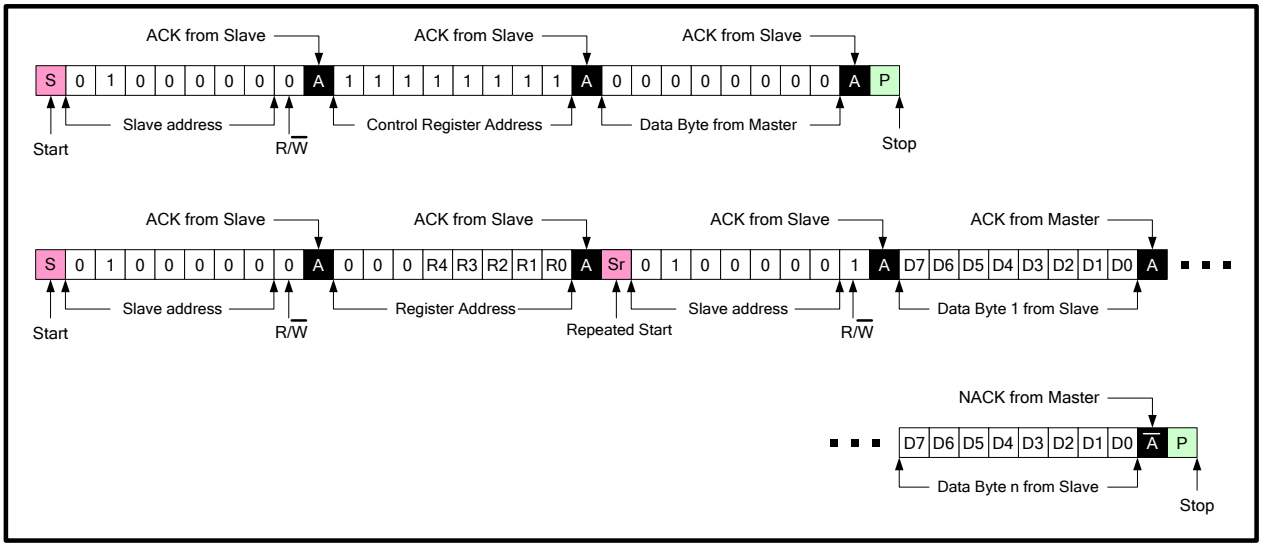
4. Write Vcom data register into EEPROM


ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 1 1 1 1 1 1 1 1 A 0 1 0 0 0 0 0 0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

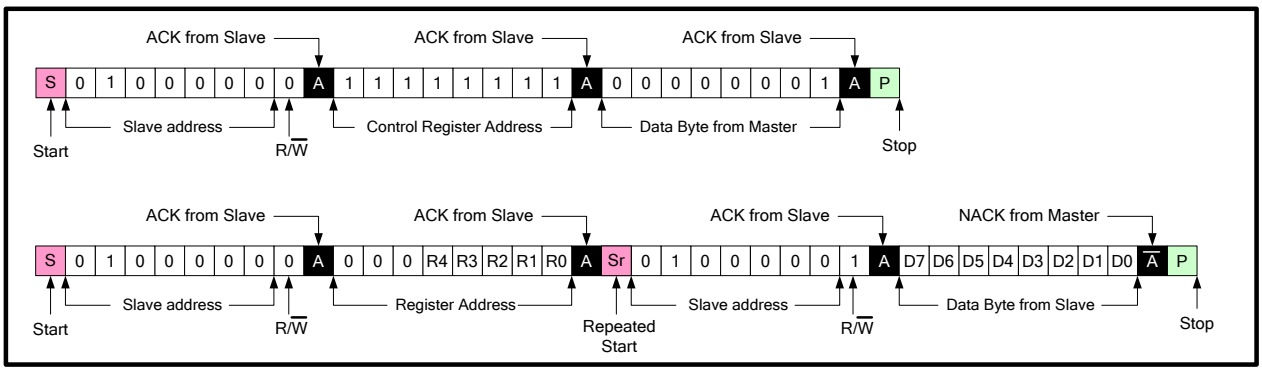
5. Read single byte of data from DAC register


ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 1 1 1 1 1 1 1 1 A 0 0 0 0 0 0 0 0 A P
Start
Slave address
R/W
Control Register Address
Data Byte from Master
Stop
ACK from Slave
ACK from Slave
ACK from Slave
NACK from Master
S 0 1 0 0 0 0 0 0 A 0 0 0 R4 R3 R2 R1 R0 A Sr 0 1 0 0 0 0 0 1 A D7 D6 D5 D4 D3 D2 D1 D0 A P
Start
Slave address
R/W
Register Address
Repeated Start
Slave address
R/W
Data Byte from Slave
Stop

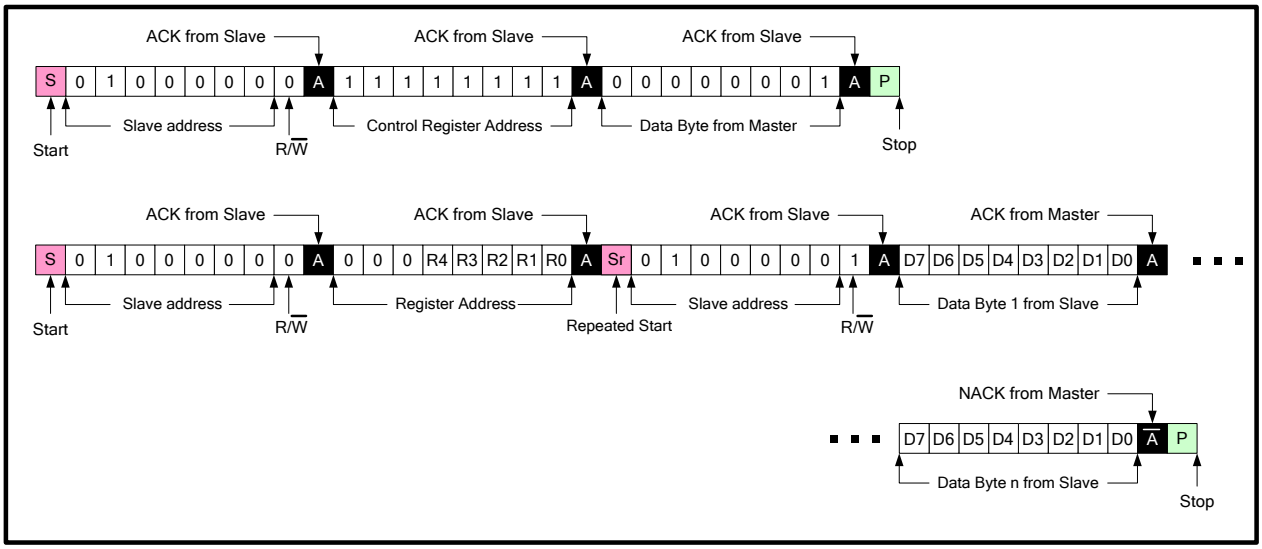
6. Read multiple bytes of data from DAC registers


ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 1 1 1 1 1 1 1 1 A 0 0 0 0 0 0 0 0 A P
Start
Slave address
R/W
Control Register Address
Data Byte from Master
Stop
ACK from Slave
ACK from Slave
ACK from Slave
ACK from Master
S 0 1 0 0 0 0 0 0 A 0 0 0 R4 R3 R2 R1 R0 A Sr 0 1 0 0 0 0 0 1 A D7 D6 D5 D4 D3 D2 D1 D0 A
Start
Slave address
R/W
Register Address
Repeated Start
Slave address
R/W
Data Byte 1 from Slave
NACK from Master
D7 D6 D5 D4 D3 D2 D1 D0 Ā P
Data Byte n from Slave
Stop

7. Read single byte of data from EEPROM

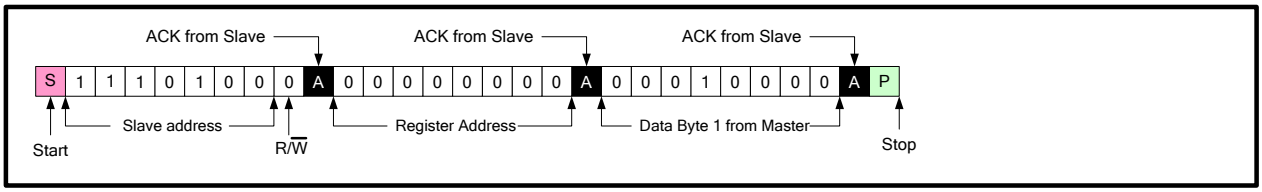

ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 1 1 1 1 1 1 1 1 A 0 0 0 0 0 0 0 1 A P
Start
Slave address
R/W
Control Register Address
Data Byte from Master
Stop
ACK from Slave
ACK from Slave
ACK from Slave
NACK from Master
S 0 1 0 0 0 0 0 0 A 0 0 0 R4 R3 R2 R1 R0 A Sr 0 1 0 0 0 0 0 1 A D7 D6 D5 D4 D3 D2 D1 D0 Ā P
Start
Slave address
R/W
Register Address
Repeated Start
Slave address
R/W
Data Byte from Slave
Stop

8. Read multiple bytes of data from EEPROM

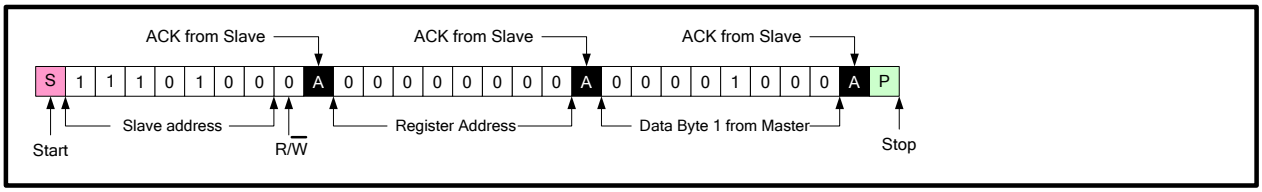

ACK from Slave
ACK from Slave
ACK from Slave
S 0 1 0 0 0 0 0 0 A 1 1 1 1 1 1 1 1 A 0 0 0 0 0 0 0 1 A P
Start
Slave address
R/W
Control Register Address
Data Byte from Master
Stop
ACK from Slave
ACK from Slave
ACK from Slave
ACK from Master
S 0 1 0 0 0 0 0 0 A 0 0 0 R4 R3 R2 R1 R0 A Sr 0 1 0 0 0 0 0 1 A D7 D6 D5 D4 D3 D2 D1 D0 A
Start
Slave address
R/W
Register Address
Repeated Start
Slave address
R/W
Data Byte 1 from Slave
NACK from Master
D7 D6 D5 D4 D3 D2 D1 D0 Ā P
Data Byte n from Slave
Stop

I2C Commend
Device address (E8h/E9h)

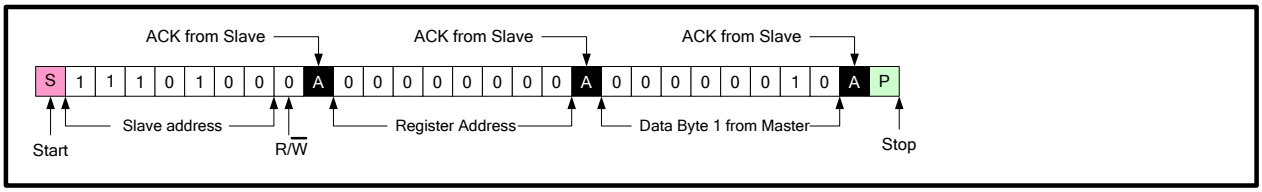
1. Load VCOM_NT EEPROM data to DAC register (RESET)


ACK from Slave
ACK from Slave
ACK from Slave
S 1 1 1 0 1 0 0 0 A 0 0 0 0 0 0 0 0 A 0 0 0 1 0 0 0 0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

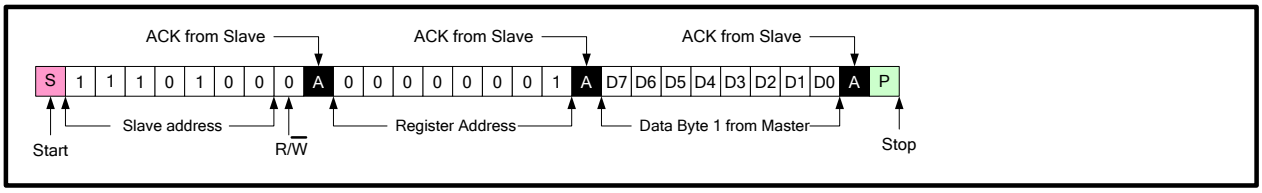
2. Write VCOM_NT DAC register into EEPROM (VCOM_NT_WR_EPM)


ACK from Slave
ACK from Slave
ACK from Slave
S 1 1 1 0 1 0 0 0 A 0 0 0 0 0 0 0 0 A 0 0 0 0 1 0 0 0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

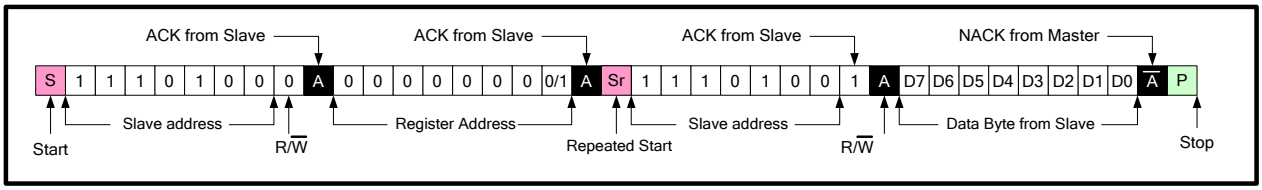
3. Set VCOM output enable=1 (OUT_EN)


ACK from Slave
ACK from Slave
ACK from Slave
S 1 1 1 0 1 0 0 0 A 0 0 0 0 0 0 0 0 A 0 0 0 0 0 0 1 0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

4. Write VCOM_NT data to DAC register


ACK from Slave
ACK from Slave
ACK from Slave
S 1 1 1 0 1 0 0 0 A 0 0 0 0 0 0 0 1 A D7 D6 D5 D4 D3 D2 D1 D0 A P
Start
Slave address
R/W
Register Address
Data Byte 1 from Master
Stop

5. Read single control byte or VCOM_NT byte of data from DAC register


ACK from Slave
ACK from Slave
ACK from Slave
NACK from Master
S 1 1 1 0 1 0 0 0 A 0 0 0 0 0 0 0 0/1 A Sr 1 1 1 0 1 0 0 1 A D7 D6 D5 D4 D3 D2 D1 D0 Ā P
Start
Slave address
R/W
Register Address
Repeated Start
Slave address
R/W
Data Byte from Slave
Stop

Register Map
Device address (40h/41h)

Address	Name	Description	Default value	Resolution	Range
00h	AVDD	[5:0] AVDD output voltage	17.6V(29h)	0.1V	@[46h] bit7=0, 13.5V(00h) to 19.8V(3Fh) @[46h] bit7=1, 11V(00h) to 17.3V(3Fh)
01h	VBK1	[4:0] VBK1 output voltage	3.3V(1Eh)	0.05V	1.8V(00h) to 3.35V(1Fh)
02h	HAVDD	[6:0] HAVDD output voltage	Res2*(64+192) (40h)	AVDD/512	Res2*(0+192), (00h) to Res2*(127+192, (7Fh) Res2= AVDD /512
03h	VGH_NT	[4:0] VGH normal temperature voltage	30V(0Ah)	1V	20V(00h) to 45V(19h)
04h	*VGH_LT_EN	[7] VGH low temperature enable	0: Disable		0: Disable 1: Enable
	VGH_LT	[4:0] VGH low temperature voltage	35V(0Fh)	1V	20V(00h) to 45V(19h)
05h	VGL_NT	[4:0] VGL normal temperature voltage	-8V(0Ah)	0.5V	-3V(00h) to -18V(1Eh)
06h	*VGL_LT/HT_EN	[7] VGL temperature compensation enable	0: Disable		0: Disable 1: Enable
	VGL_LT/HT_SEL	[6] VGL low or high temperature compensation selection	0:VGL_LT		0:VGL_LT 1:VGL_HT
	VGL_LT/HT	[4:0] VGL low temperature voltage / VGL high temperature voltage	-12V(12h)	0.5V	-3V(00h) to –18V(1Eh)
07h	*VCOM1_HT_EN	[7] VCOM1 high temperature enable	0: Disable		0: Disable 1: Enable
	VSS1	[4:0] VSS1 output voltage	-6(06h)	0.5V	-3V(00h) to -16V(1Ah)
08h	VCOM1_NT	[7:1] VCOM1_NT normal temperature voltage	63*Res1+VCOMMIN (7Eh)	Res1	VCOM_MIN to VCOM_MAX Res1=(VCOM_MAX-VCOM_MIN)/127
09h	VCOM1_HT	[7:1] VCOM1 high temperature voltage	93*Res1+VCOM_MIN (BAh)	Res1	VCOM_MIN to VCOM_MAX Res1=(VCOM_MAX-VCOM_MIN)/127
0Ah	VCOM_MAX	[6:0] VCOM1 & VCOM2DAC high limit voltage	64*Res3 (3Fh)	Res3	1*Res1(00h) to 128*Res1(7Fh) Res3= V_{AVDD} /128
0Bh	VCOM_MIN	[6:0] VCOM1 & VCOM2DAC low limit voltage	38*Res3 (26h)	Res3	0*Res1(00h) to 127*Res1(7Fh) Res3= V_{AVDD} /128
0Ch	**GAMMA1	[9:0] Gamma1 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
0Dh					
0Eh	**GAMMA2	[9:0] Gamma2 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
0Fh					
10h	**GAMMA3	[9:0] Gamma3 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
11h					
12h	**GAMMA4	[9:0] Gamma4 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
13h					
14h	**GAMMA5	[9:0] Gamma5 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
15h					
16h	**GAMMA6	[9:0] Gamma6 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
17h					
18h	**GAMMA7	[9:0] Gamma7 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
19h					
1Ah	**GAMMA8	[9:0] Gamma8 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
1Bh					

Register Map
Device address (40h/41h)

Address	Name	Description	Default value	Resolution	Range
1Ch 1Dh	**GAMMA9	[9:0] Gamma9 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
1Eh 1Fh	**GAMMA10	[9:0] Gamma10 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
20h 21h	**GAMMA11	[9:0] Gamma11 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
22h 23h	**GAMMA12	[9:0] Gamma12 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
24h 25h	**GAMMA13	[9:0] Gamma13 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
26h 27h	**GAMMA14	[9:0] Gamma14 output voltage	512*Res4 (200h)	Res4	0V(000h) to V_{AVDD}(3FFh) Res4=V_{AVDD} /1024
28h	Group B_EN	[7] Group B enable (Group B: AVDD, HAVDD, VGH, VGL, VSS1/2, Gamma, VCOM1, VCOM2 DAC, L/S output)	0: Disable		0: Disable 1: Enable
	VGL_EN	[6] VGL enable	1: Enable		0: Disable 1: Enable
	VSS1_EN	[5] VSS1 enable	1: Enable		0: Disable 1: Enable
	AVDD_EN	[4] AVDD enable	1: Enable		0: Disable 1: Enable
	HAVDD_EN	[3] HAVDD enable	1: Enable		0: Disable 1: Enable
	GMA_EN	[2] Gamma enable	1: Enable		0: Disable 1: Enable
	VCOM1_EN	[1] VCOM1 enable	1: Enable		0: Disable 1: Enable
	VGH_EN	[0] VGH enable	1: Enable		0: Disable 1: Enable
29h	FREQ_SEL	[7] Frequency select	0: 750kHz		0: 750kHz 1:500kHz
	AVDD_NMOS_INT/EXT	[4] AVDD NMOS_ Internal / External	0: Internal		0: Internal 1: External (@[2Ah] bit3 output keep Boost and bit1 output keep LXBK1)
	VGH_TYPE	[3] VGH structure type	0: Boost		0: Boost 1: Charge pump (AVDD internal mode only)
	VGL_TYPE	[2] VGL structure type	0: Inverting		0: Inverting 1: Charge pump (AVDD internal mode or AVDD external & LXBK1 only)
	VGL_PUMP_SOURCE	[1] VGL charge pump source	0: VBK1		0: LXBK1 1: LX/CS
	GMA_CH_TYPE	[0] Gamma channel type	0: 14_CH		0: 14_CH (1 to 14_CH) 1: 4_CH (1,7,8,14_CH)
2Ah	DLY1_VBK1	[5:4] Delay1_VBK1	00 : 0ms		@[46h] bit7=0, 00: 0ms 01: 2ms 10: 4ms 11: 6ms @[46h] bit7=1, 00: 0ms 01: 40ms 10: 80ms 11: 120ms
	DLY2_VGL	[3:2] Delay2_VGL	01 : 5ms		00: 0ms 01: 5ms 10: 10ms 11: 15ms
	DLY3_VSS1	[1:0] Delay3_VSS1	01 : 2ms		00: 0ms 01: 2ms 10: 4ms 11: 6ms

Register Map
Device address (40h/41h)

Address	Name	Description	Default value	Resolution	Range
2Bh	DLY4_AVDD	[6:5] Delay4_AVDD	01: 5ms		00: 0ms 01:5ms 10: 10ms 11: 15ms
	DLY5_VGH	[4:3] Delay5_VGH	01: 2ms		00: 0ms 01:2ms 10: 4ms 11: 6ms
	DLY6_VCOM	[2:0] Delay6_VCOM1 & VCOM2 DAC	000: 0ms		000: 0ms 001: 30ms 010: 60ms 011: 90ms 100: 120ms 101: 150ms 110: 180ms 111:210ms
2Ch	ALL_DIS_EN	[7] All discharge enable	1: Enable		0: Disable 1: Enable
	BK1_DIS	[6] Buck1 discharge	1: 1kohm		0: 0.5kohm 1: 1kohm
	AVDD_DIS	[5] AVDD discharge	1: 4.7kohm		0: 1.4kohm 1: 4.7kohm
	VGH_DIS	[4] VGH discharge	1: 30kohm		0: 1.5kohm 1: 30kohm
	VGL_DIS	[3] VGL discharge enable	1: 10kohm		0: Disable 1: 10kohm
	HAVDD_DIS	[2] HAVDD discharge enable	1: 10kohm		0: Disable 1: 10kohm
	VCOM1_DIS	[1:0] VCOM1 discharge enable	11: 8kohm		00: Disable 01:20 ohm 10: 1k ohm 11:8kohm
2Dh	VSS1_DIS	[7] VSS1 discharge enable	1: 1.2kohm		0: Disable 1: 1.2kohm
	VCOM1_DIS_TYP	[4] VCOM1 discharge type	0: VIN_UVOL_F		0: VIN_VULO_F 1: XON discharge threshold
	HAVDD_FB	[3] HAVDD feedback mode select	0: (G7+G8)/2		0: (G7+G8)/2 1:HAVDD DAC register
	AVDD_GD_SC	[2] AVDD GDMOS SCP select	0: GD_SC_Mode1		0:GD_SC_Mode1 (power-up of three fail attempts) 1:GD_SC_Mode2 (power-up of three fail attempts and AVDD FIMV detect)
	AVDD_SS	[1] AVDD soft start	0: 10ms		0:10ms 1: 20ms
	VGH_SS	[0] VGH soft start	1: 6ms		0:3ms 1: 6ms
2Eh	VGH&VGL_VTC1/2	[7:4] VGH&VGL_VTC2	1101: 3.0V	0.2V	0000: 0.4V to 1111: 3.4V
		[3:0] VGH&VGL_VTC1	1000: 2.0V	0.2V	0000: 0.4V to 1111: 3.4V
2Fh	VCOM1_VTC1/2	[7:4] VCOM1_VTC2	0100: 1.2V	0.2V	0000: 0.4V to 1111: 3.4V
		[3:0] VCOM1_VTC1	0001: 0.6V	0.2V	0000: 0.4V to 1111: 3.4V
30h	AVDD_EXT_DRV	[5:4] AVDD external driving of Gate	01: EXT_DRV2_F		00: EXT_DRV1_FF 01: EXT_DRV2_F 10: EXT_DRV3_S 11: EXT_DRV4_SS
	VGH_Boost_COMP	[3:2] VGH boost converter compensation	10:VGH_COMP3_S		00: VGH_COMP1_FF 01: VGH_COMP2_F 10: VGH_COMP3_S 11: VGH_COMP4_SS
	VGL_Inverting_COMP	[1:0] VGL inverting compensation	10:VGL_COMP3_S		00: VGL_COMP1_FF 01: VGL_COMP2_F 10: VGL_COMP3_S 11: VGL_COMP4_SS

Register Map
Device address (40h/41h)

Address	Name	Description	Default value	Resolution	Range
31h	EN_PIN_SEL	[7] EN pin function select	0		0: EN input function 1: XON output function
	VCOM1_DLY_OFF	[6] VCOM1 delay power off	0		0: Disable 1: Enable
	HAVDD_DLY_OFF	[5] HAVDD delay power off	0		0: Disable 1: Enable
	GMA_DLY_OFF	[4] Gamma1~14 delay power off	0		0: Disable 1: Enable
	XON_DIS_THR	[3:0] XON discharge threshold	0010: 7V	0.25V	@[46h] bit7=0, 6.50V(00h) to 10.25V(0Fh) 0000: 6.50V 0001:6.75V 0010: 7.00V 0011:7.25V 0100: 7.50V 0101:7.75V 0110: 8.00V 0111:8.25V 1000: 8.50V 1001:8.75V 1010:9.00V 1011:9.25V 1100:9.50V 1101:9.75V 1110:10.00V 1111:10.25V @[46h] bit7=1, 3.63V(00h) to VINUV(0Fh) 0000: 3.63V 0001: 3.77V 0010: 3.91V 0011: 4.05V 0100: 4.19V 0101: 4.33V 0110: 4.47V 0111: 4.60V 1000: 4.74V 1001: 4.88V 1010: 5.02V 1011: 5.16V 1100: 5.30V 1101: 5.44V 1110:5.58V 1111: VINUV
32h~44h	-	Reserved	---	---	---
45h	VCOM2DAC	[7:1] VCOM2DAC normal temperature voltage	63*Res1+VCOMMIN (7Eh)	Res1	VCOM_MIN to VCOM_MAX Res1=(VCOM_MAX-VCOM_MIN)/127
	-	[0]Reserved	---	---	---
46h	MNT_MODE_EN-	[7]MNT MODE select	1	---	0 : TV MODE (VIN=12V) 1 : MNT MODE (VIN=5V)
		[6:1]Reserved	---	---	---
	VCOM2DAC_EN	[0] VCOM2DAC enable	0: Disable	---	0: Disable 1:Enable
FFh	***CR	[7;6] & [0] Control register			00h, 01h, 40h, 80h
		[1] GMT use			GMT flag for internal use only

*VGH, VGL and VCOM1 temperature compensation

(a) VGH, VGL and VCOM1 temperature compensation enable can be setting by 04h[7], 06h[7] and 07h[7]
(b) VGL_LT (positive compensation) or VGL_HT (negative compensation) can be selection by 06h[6]

**GAMMA register map

Address	Name	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	GAMMA1	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA1[9:8]	
0Dh	GAMMA1	00h	GMA1[7:0]							
0Eh	GAMMA2	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA2[9:8]	
0Fh	GAMMA2	00h	GMA2[7:0]							
……	……	……	……	……	……	……	……	……	……	
……	……	……	……							
……	……	……	……	……	……	……	……	……	……	
……	……	……	……							
24h	GAMMA13	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA13[9:8]	
25h	GAMMA13	00h	GMA13[7:0]							
26h	GAMMA14	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA14[9:8]	
27h	GAMMA14	00h	GMA14[7:0]							

***Control Register (with factory value) — FFh, (00h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
W_ALL	W_VCOM1	Reserved	Reserved	Reserved	Reserved	GMT use	EE/DR

DAC value	Control register description
00h	00h : Read data from DAC register.
01h	01h : Read data from EEPROM.
40h	40h : Write VCOM1 data from DAC register to EEPROM.
80h	80h : Write all data from DAC register to EEPROM.

AVDD output voltage (with factory value) — 00h, (29h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	1	0	1	0	0	1

※MNT_MODE_EN @46H[7]=0

DAC value	AVDD	DAC value	AVDD	DAC value	AVDD	DAC value	AVDD
00h	13.5V	10h	15.1V	20h	16.7V	30h	18.3V
01h	13.6V	11h	15.2V	21h	16.8V	31h	18.4V
02h	13.7V	12h	15.3V	22h	16.9V	32h	18.5V
03h	13.8V	13h	15.4V	23h	17.0V	33h	18.6V
04h	13.9V	14h	15.5V	24h	17.1V	34h	18.7V
05h	14.0V	15h	15.6V	25h	17.2V	35h	18.8V
06h	14.1V	16h	15.7V	26h	17.3V	36h	18.9V
07h	14.2V	17h	15.8V	27h	17.4V	37h	19.0V
08h	14.3V	18h	15.9V	28h	17.5V	38h	19.1V
09h	14.4V	19h	16.0V	29h	17.6V	39h	19.2V
0Ah	14.5V	1Ah	16.1V	2Ah	17.7V	3Ah	19.3V
0Bh	14.6V	1Bh	16.2V	2Bh	17.8V	3Bh	19.4V
0Ch	14.7V	1Ch	16.3V	2Ch	17.9V	3Ch	19.5V
0Dh	14.8V	1Dh	16.4V	2Dh	18.0V	3Dh	19.6V
0Eh	14.9V	1Eh	16.5V	2Eh	18.1V	3Eh	19.7V
0Fh	15.0V	1Fh	16.6V	2Fh	18.2V	3Fh	19.8V

※MNT_MODE_EN @46H[7]=1

DAC value	AVDD	DAC value	AVDD	DAC value	AVDD	DAC value	AVDD
00h	11	10h	12.6	20h	14.2	30h	15.8
01h	11.1	11h	12.7	21h	14.3	31h	15.9
02h	11.2	12h	12.8	22h	14.4	32h	16
03h	11.3	13h	12.9	23h	14.5	33h	16.1
04h	11.4	14h	13	24h	14.6	34h	16.2
05h	11.5	15h	13.1	25h	14.7	35h	16.3
06h	11.6	16h	13.2	26h	14.8	36h	16.4
07h	11.7	17h	13.3	27h	14.9	37h	16.5
08h	11.8	18h	13.4	28h	15	38h	16.6
09h	11.9	19h	13.5	29h	15.1	39h	16.7
0Ah	12	1Ah	13.6	2Ah	15.2	3Ah	16.8
0Bh	12.1	1Bh	13.7	2Bh	15.3	3Bh	16.9
0Ch	12.2	1Ch	13.8	2Ch	15.4	3Ch	17
0Dh	12.3	1Dh	13.9	2Dh	15.5	3Dh	17.1
0Eh	12.4	1Eh	14	2Eh	15.6	3Eh	17.2
0Fh	12.5	1Fh	14.1	2Fh	15.7	3Fh	17.3

VBK1 output voltage (with factory value) — 01h, (1Eh)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	1	1	1	1	0

DAC value	VBK1	DAC value	VBK1	DAC value	VBK1	DAC value	VBK1
00h	1.80V	08h	2.20V	10h	2.60V	18h	3.00V
01h	1.85V	09h	2.25V	11h	2.65V	19h	3.05V
02h	1.90V	0Ah	2.30V	12h	2.70V	1Ah	3.10V
03h	1.95V	0Bh	2.35V	13h	2.75V	1Bh	3.15V
04h	2.00V	0Ch	2.40V	14h	2.80V	1Ch	3.20V
05h	2.05V	0Dh	2.45V	15h	2.85V	1Dh	3.25V
06h	2.10V	0Eh	2.50V	16h	2.90V	1Eh	3.30V
07h	2.15V	0Fh	2.55V	17h	2.95V	1Fh	3.35V

HAVDD output voltage (with factory value) — 03h, (40h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	1	0	0	0	0	0	0

HAVDD voltage formula
HAVDD=Res2 *(HAVDD_CODE+192)
Res2 = AVDD / 512
HAVDD_CODE= 0 ~ 127

HAVDD output voltage (Unit: V)

DAC value	HAVDD	DAC value	HAVDD	DAC value	HAVDD	DAC value	HAVDD	DAC value	HAVDD
00h	Res2*(0+192)	1Ah	Res2*(26+192)	34h	Res2*(52+192)	4Eh	Res2*(78+192)	68h	Res2*(104+192)
01h	Res2*(1+192)	1Bh	Res2*(27+192)	35h	Res2*(53+192)	4Fh	Res2*(79+192)	69h	Res2*(105+192)
02h	Res2*(2+192)	1Ch	Res2*(28+192)	36h	Res2*(54+192)	50h	Res2*(80+192)	6Ah	Res2*(106+192)
03h	Res2*(3+192)	1Dh	Res2*(29+192)	37h	Res2*(55+192)	51h	Res2*(81+192)	6Bh	Res2*(107+192)
04h	Res2*(4+192)	1Eh	Res2*(30+192)	38h	Res2*(56+192)	52h	Res2*(82+192)	6Ch	Res2*(108+192)
05h	Res2*(5+192)	1Fh	Res2*(31+192)	39h	Res2*(57+192)	53h	Res2*(83+192)	6Dh	Res2*(109+192)
06h	Res2*(6+192)	20h	Res2*(32+192)	3Ah	Res2*(58+192)	54h	Res2*(84+192)	6Eh	Res2*(110+192)
07h	Res2*(7+192)	21h	Res2*(33+192)	3Bh	Res2*(59+192)	55h	Res2*(85+192)	6Fh	Res2*(111+192)
08h	Res2*(8+192)	22h	Res2*(34+192)	3Ch	Res2*(60+192)	56h	Res2*(86+192)	70h	Res2*(112+192)
09h	Res2*(9+192)	23h	Res2*(35+192)	3Dh	Res2*(61+192)	57h	Res2*(87+192)	71h	Res2*(113+192)
0Ah	Res2*(10+192)	24h	Res2*(36+192)	3Eh	Res2*(62+192)	58h	Res2*(88+192)	72h	Res2*(114+192)
0Bh	Res2*(11+192)	25h	Res2*(37+192)	3Fh	Res2*(63+192)	59h	Res2*(89+192)	73h	Res2*(115+192)
0Ch	Res2*(12+192)	26h	Res2*(38+192)	40h	Res2*(64+192)	5Ah	Res2*(90+192)	74h	Res2*(116+192)
0Dh	Res2*(13+192)	27h	Res2*(39+192)	41h	Res2*(65+192)	5Bh	Res2*(91+192)	75h	Res1*(117+192)
0Eh	Res2*(14+192)	28h	Res2*(40+192)	42h	Res2*(66+192)	5Ch	Res2*(92+192)	76h	Res2*(118+192)
0Fh	Res2*(15+192)	29h	Res2*(41+192)	43h	Res2*(67+192)	5Dh	Res2*(93+192)	77h	Res2*(119+192)
10h	Res2*(16+192)	2Ah	Res2*(42+192)	44h	Res2*(68+192)	5Eh	Res2*(94+192)	78h	Res2*(120+192)
11h	Res2*(17+192)	2Bh	Res2*(43+192)	45h	Res2*(69+192)	5Fh	Res2*(95+192)	79h	Res2*(121+192)
12h	Res2*(18+192)	2Ch	Res2*(44+192)	46h	Res2*(70+192)	60h	Res2*(96+192)	7Ah	Res2*(122+192)
13h	Res2*(19+192)	2Dh	Res2*(45+192)	47h	Res2*(71+192)	61h	Res2*(97+192)	7Bh	Res2*(123+192)
14h	Res2*(20+192)	2Eh	Res2*(46+192)	48h	Res2*(72+192)	62h	Res2*(98+192)	7Ch	Res2*(124+192)
15h	Res2*(21+192)	2Fh	Res2*(47+192)	49h	Res2*(73+192)	63h	Res2*(99+192)	7Dh	Res2*(125+192)
16h	Res2*(22+192)	30h	Res2*(48+192)	4Ah	Res2*(74+192)	64h	Res2*(100+192)	7Eh	Res2*(126+192)
17h	Res2*(23+192)	31h	Res2*(49+192)	4Bh	Res2*(75+192)	65h	Res2*(101+192)	7Fh	Res2*(127+192)
18h	Res2*(24+192)	32h	Res2*(50+192)	4Ch	Res2*(76+192)	66h	Res2*(102+192)		
19h	Res2*(25+192)	33h	Res2*(51+192)	4Dh	Res2*(77+192)	67h	Res2*(103+192)		

VGH_NT output voltage (with factory value) — 03h, (0Ah)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	0	1	0	1	0

DAC value	VGH_NT	DAC value	VGH_NT	DAC value	VGH_NT	DAC value	VGH_NT
00h	20V	08h	28V	10h	36V	18h	44V
01h	21V	09h	29V	11h	37V	19h	45V
02h	22V	0Ah	30V	12h	38V		
03h	23V	0Bh	31V	13h	39V		
04h	24V	0Ch	32V	14h	40V		
05h	25V	0Dh	33V	15h	41V		
06h	26V	0Eh	34V	16h	42V		
07h	27V	0Fh	35V	17h	43V		

VGH_LT output voltage (with factory value) — 04h, (0Fh)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGH_LT_EN	--	--	VGH_LT[4:0]				
0	Reserved	Reserved	0	1	1	1	1

Bit	Name	Description
Bit7	VGH_LT_EN	VGH temperature compensation enable 0: Disable 1: Enable

DAC value	VGH_LT	DAC value	VGH_LT	DAC value	VGH_LT	DAC value	VGH_LT
00h	20V	08h	28V	10h	36V	18h	44V
01h	21V	09h	29V	11h	37V	19h	45V
02h	22V	0Ah	30V	12h	38V		
03h	23V	0Bh	31V	13h	39V		
04h	24V	0Ch	32V	14h	40V		
05h	25V	0Dh	33V	15h	41V		
06h	26V	0Eh	34V	16h	42V		
07h	27V	0Fh	35V	17h	43V		

VGL_NT output voltage (with factory value) — 05h, (0Ah)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	0	1	0	1	0

DAC value	VGL_NT	DAC value	VGL_NT	DAC value	VGL_NT	DAC value	VGL_NT
00h	-3.0V	08h	-7.0V	10h	-11.0V	18h	-15.0V
01h	-3.5V	09h	-7.5V	11h	-11.5V	19h	-15.5V
02h	-4.0V	0Ah	-8.0V	12h	-12.0V	1Ah	-16.0V
03h	-4.5V	0Bh	-8.5V	13h	-12.5V	1Bh	-16.5V
04h	-5.0V	0Ch	-9.0V	14h	-13.0V	1Ch	-17.0V
05h	-5.5V	0Dh	-9.5V	15h	-13.5V	1Dh	-17.5V
06h	-6.0V	0Eh	-10.0V	16h	-14.0V	1Eh	-18.0V
07h	-6.5V	0Fh	-10.5V	17h	-14.5V		

VGL_LT/HT output voltage (with factory value) — 06h, (12h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VGL_LT/HT_EN	VGL_LT/HT_SEL	--	VGL_LT/HT[4:0]				
0	0	Reserved	0	1	1	0	0

Bit	Name	Description
Bit7	VGL_LT/HT_EN	VGL_LT/HT temperature compensation enable 0: Disable 1: Enable
Bit6	VGL_LT/HT_SEL	VGL_LT/HT temperature compensation select 0: VGL_LT 1: VGL_HT

DAC value	VGL_LT/HT	DAC value	VGL_LT/HT	DAC value	VGL_LT/HT	DAC value	VGL_LT/HT
00h	-3.0V	08h	-7.0V	10h	-11.0V	18h	-15.0V
01h	-3.5V	09h	-7.5V	11h	-11.5V	19h	-15.5V
02h	-4.0V	0Ah	-8.0V	12h	-12.0V	1Ah	-16.0V
03h	-4.5V	0Bh	-8.5V	13h	-12.5V	1Bh	-16.5V
04h	-5.0V	0Ch	-9.0V	14h	-13.0V	1Ch	-17.0V
05h	-5.5V	0Dh	-9.5V	15h	-13.5V	1Dh	-17.5V
06h	-6.0V	0Eh	-10.0V	16h	-14.0V	1Eh	-18.0V
07h	-6.5V	0Fh	-10.5V	17h	-14.5V		

VCOM1_HT_EN & VSS1 output voltage (with factory value) — 07h, (06h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Reserved	Reserved	0	0	1	1	0

Bit	Name	Description
Bit7	VCOM1_HT_EN	VCOM1_HT temperature compensation enable 0: Disable 1: Enable

VSS1 [4:0]							
DAC value	VSS1	DAC value	VSS1	DAC value	VSS1	DAC value	VSS1
00h	-3.0V	08h	-7.0V	10h	-11.0V	18h	-15.0V
01h	-3.5V	09h	-7.5V	11h	-11.5V	19h	-15.5V
02h	-4.0V	0Ah	-8.0V	12h	-12.0V	1Ah	-16.0V
03h	-4.5V	0Bh	-8.5V	13h	-12.5V		
04h	-5.0V	0Ch	-9.0V	14h	-13.0V		
05h	-5.5V	0Dh	-9.5V	15h	-13.5V		
06h	-6.0V	0Eh	-10.0V	16h	-14.0V		
07h	-6.5V	0Fh	-10.5V	17h	-14.5V		

VCOM1_NT (with factory value) — 08h, (7Eh)
VCOM1_HT (with factory value) — 09h, (BAh)
VCOM_MAX (with factory value) — 0Ah, (3Fh)
VCOM_MIN (with factory value) — 0Bh, (26h)

Address	Name	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	VCOM1_NT	7Eh	0	1	1	1	1	1	1	Reserved
09h	VCOM1_HT	BAh	1	0	1	1	1	0	1	Reserved
0Ah	VCOM_MAX	3Fh	Reserved	0	1	0	0	1	1	0
0Bh	VCOM_MIN	26h	Reserved	0	1	1	1	1	1	1

VCOM1_NT voltage formula
VCOM1_NT=Res1*VCOM1_NT CODE +VCOM_MIN
Res1=(VCOMMAX-VCOM_MIN)/127 ; VCOM1_NT CODE= 0 ~ 127

VCOM1_HT voltage formula
VCOM1_HT= Res1*VCOM1_HT CODE +VCOM_MIN
Res1=(VCOM_MAX-VCOM_MIN)/127 ; VCOM1_HT CODE= 0 ~ 127

VCOM_MAX/VCOM_MIN voltage formula
VCOM_MAX=Res3 * [(VCOM_MAX_CODE)+1]
VCOM_MIN=Res3 * VCOM_MIN_CODE
Res3 = V_{AVDD} / 128

VCOM1_NT / VCOM1_HT output voltage (Unit: V)

DAC value	VCOM_NT / VCOM_HT	DAC value	VCOM_NT / VCOM_HT
00h	Res1*0+VCOM_MIN	80h	Res1*64+VCOM_MIN
02h	Res1*1+VCOM_MIN	82h	Res1*65+VCOM_MIN
04h	Res1*2+VCOM_MIN	84h	Res1*66+VCOM_MIN
06h	Res1*3+VCOM_MIN	86h	Res1*67+VCOM_MIN
08h	Res1*4+VCOM_MIN	88h	Res1*68+VCOM_MIN
0Ah	Res1*5+VCOM_MIN	8Ah	Res1*69+VCOM_MIN
0Ch	Res1*6+VCOM_MIN	8Ch	Res1*70+VCOM_MIN
0Eh	Res1*7+VCOM_MIN	8Eh	Res1*71+VCOM_MIN
10h	Res1*8+VCOM_MIN	90h	Res1*72+VCOM_MIN
12h	Res1*9+VCOM_MIN	92h	Res1*73+VCOM_MIN
14h	Res1*10+VCOM_MIN	94h	Res1*74+VCOM_MIN
16h	Res1*11+VCOM_MIN	96h	Res1*75+VCOM_MIN
18h	Res1*12+VCOM_MIN	98h	Res1*76+VCOM_MIN
1Ah	Res1*13+VCOM_MIN	9Ah	Res1*77+VCOM_MIN
1Ch	Res1*14+VCOM_MIN	9Ch	Res1*78+VCOM_MIN
1Eh	Res1*15+VCOM_MIN	9Eh	Res1*79+VCOM_MIN
20h	Res1*16+VCOM_MIN	A0h	Res1*80+VCOM_MIN
22h	Res1*17+VCOM_MIN	A2h	Res1*81+VCOM_MIN
24h	Res1*18+VCOM_MIN	A4h	Res1*82+VCOM_MIN
26h	Res1*19+VCOM_MIN	A6h	Res1*83+VCOM_MIN
28h	Res1*20+VCOM_MIN	A8h	Res1*84+VCOM_MIN
2Ah	Res1*21+VCOM_MIN	AAh	Res1*85+VCOM_MIN
2Ch	Res1*22+VCOM_MIN	ACh	Res1*86+VCOM_MIN
2Eh	Res1*23+VCOM_MIN	AEh	Res1*87+VCOM_MIN
30h	Res1*24+VCOM_MIN	B0h	Res1*88+VCOM_MIN
32h	Res1*25+VCOM_MIN	B2h	Res1*89+VCOM_MIN
34h	Res1*26+VCOM_MIN	B4h	Res1*90+VCOM_MIN
36h	Res1*27+VCOM_MIN	B6h	Res1*91+VCOM_MIN
38h	Res1*28+VCOM_MIN	B8h	Res1*92+VCOM_MIN
3Ah	Res1*29+VCOM_MIN	**BAh**	**Res1*93+VCOM_MIN**
3Ch	Res1*30+VCOM_MIN	BCh	Res1*94+VCOM_MIN
3Eh	Res1*31+VCOM_MIN	BEh	Res1*95+VCOM_MIN
40h	Res1*32+VCOM_MIN	C0h	Res1*96+VCOM_MIN
42h	Res1*33+VCOM_MIN	C2h	Res1*97+VCOM_MIN
44h	Res1*34+VCOM_MIN	C4h	Res1*98+VCOM_MIN
46h	Res1*35+VCOM_MIN	C6h	Res1*99+VCOM_MIN
48h	Res1*36+VCOM_MIN	C8h	Res1*100+VCOM_MIN
4Ah	Res1*37+VCOM_MIN	CAh	Res1*101+VCOM_MIN
4Ch	Res1*38+VCOM_MIN	CCh	Res1*102+VCOM_MIN
4Eh	Res1*39+VCOM_MIN	CEh	Res1*103+VCOM_MIN
50h	Res1*40+VCOM_MIN	D0h	Res1*104+VCOM_MIN
52h	Res1*41+VCOM_MIN	D2h	Res1*105+VCOM_MIN
54h	Res1*42+VCOM_MIN	D4h	Res1*106+VCOM_MIN
56h	Res1*43+VCOM_MIN	D6h	Res1*107+VCOM_MIN
58h	Res1*44+VCOM_MIN	D8h	Res1*108+VCOM_MIN
5Ah	Res1*45+VCOM_MIN	DAh	Res1*109+VCOM_MIN
5Ch	Res1*46+VCOM_MIN	DCh	Res1*110+VCOM_MIN
5Eh	Res1*47+VCOM_MIN	DEh	Res1*111+VCOM_MIN
60h	Res1*48+VCOM_MIN	E0h	Res1*112+VCOM_MIN
62h	Res1*49+VCOM_MIN	E2h	Res1*113+VCOM_MIN
64h	Res1*50+VCOM_MIN	E4h	Res1*114+VCOM_MIN
66h	Res1*51+VCOM_MIN	E6h	Res1*115+VCOM_MIN
68h	Res1*52+VCOM_MIN	E8h	Res1*116+VCOM_MIN
6Ah	Res1*53+VCOM_MIN	FAh	Res1*117+VCOM_MIN
6Ch	Res1*54+VCOM_MIN	FCh	Res1*118+VCOM_MIN
6Eh	Res1*55+VCOM_MIN	FEh	Res1*119+VCOM_MIN
70h	Res1*56+VCOM_MIN	F0h	Res1*120+VCOM_MIN
72h	Res1*57+VCOM_MIN	F2h	Res1*121+VCOM_MIN
74h	Res1*58+VCOM_MIN	F4h	Res1*122+VCOM_MIN
76h	Res1*59+VCOM_MIN	F6h	Res1*123+VCOM_MIN
78h	Res1*60+VCOM_MIN	F8h	Res1*124+VCOM_MIN
7Ah	Res1*61+VCOM_MIN	FAh	Res1*125+VCOM_MIN
7Ch	Res1*62+VCOM_MIN	FCh	Res1*126+VCOM_MIN
7Eh	**Res1*63+VCOM_MIN**	FEh	Res1*127+VCOM_MIN

Res1=(VCOMMAX-VCOM_MIN)/127

VCOM_MAX / VCOM_MIN output voltage (Unit: V)

DAC value	VCOM_MAX	VCOM_MIN	DAC value	VCOM_MAX	VCOM_MIN
00h	Res3*1	Res3*0	40h	Res3*65	Res3*64
01h	Res3*2	Res3*1	41h	Res3*66	Res3*65
02h	Res3*3	Res3*2	42h	Res3*67	Res3*66
03h	Res3*4	Res3*3	43h	Res3*68	Res3*67
04h	Res3*5	Res3*4	44h	Res3*69	Res3*68
05h	Res3*6	Res3*5	45h	Res3*70	Res3*69
06h	Res3*7	Res3*6	46h	Res3*71	Res3*70
07h	Res3*8	Res3*7	47h	Res3*72	Res3*71
08h	Res3*9	Res3*8	48h	Res3*73	Res3*72
09h	Res3*10	Res3*9	49h	Res3*74	Res3*73
0Ah	Res3*11	Res3*10	4Ah	Res3*75	Res3*74
0Bh	Res3*12	Res3*11	4Bh	Res3*76	Res3*75
0Ch	Res3*13	Res3*12	4Ch	Res3*77	Res3*76
0Dh	Res3*14	Res3*13	4Dh	Res3*78	Res3*77
0Eh	Res3*15	Res3*14	4Eh	Res3*79	Res3*78
0Fh	Res3*16	Res3*15	4Fh	Res3*80	Res3*79
10h	Res3*17	Res3*16	50h	Res3*81	Res3*80
11h	Res3*18	Res3*17	51h	Res3*82	Res3*81
12h	Res3*19	Res3*18	52h	Res3*83	Res3*82
13h	Res3*20	Res3*19	53h	Res3*84	Res3*83
14h	Res3*21	Res3*20	54h	Res3*85	Res3*84
15h	Res3*22	Res3*21	55h	Res3*86	Res3*85
16h	Res3*23	Res3*22	56h	Res3*87	Res3*86
17h	Res3*24	Res3*23	57h	Res3*88	Res3*87
18h	Res3*25	Res3*24	58h	Res3*89	Res3*88
19h	Res3*26	Res3*25	59h	Res3*90	Res3*89
1Ah	Res3*27	Res3*26	5Ah	Res3*91	Res3*90
1Bh	Res3*28	Res3*27	5Bh	Res3*92	Res3*91
1Ch	Res3*29	Res3*28	5Ch	Res3*93	Res3*92
1Dh	Res3*30	Res3*29	5Dh	Res3*94	Res3*93
1Eh	Res3*31	Res3*30	5Eh	Res3*95	Res3*94
1Fh	Res3*32	Res3*31	5Fh	Res3*96	Res3*95
20h	Res3*33	Res3*32	60h	Res3*97	Res3*96
21h	Res3*34	Res3*33	61h	Res3*98	Res3*97
22h	Res3*35	Res3*34	62h	Res3*99	Res3*98
23h	Res3*36	Res3*35	63h	Res3*100	Res3*99
24h	Res3*37	Res3*36	64h	Res3*101	Res3*100
25h	Res3*38	Res3*37	65h	Res3*102	Res3*101
26h	Res3*39	**Res3*38**	66h	Res3*103	Res3*102
27h	Res3*40	Res3*39	67h	Res3*104	Res3*103
28h	Res3*41	Res3*40	68h	Res3*105	Res3*104
29h	Res3*42	Res3*41	69h	Res3*106	Res3*105
2Ah	Res3*43	Res3*42	6Ah	Res3*107	Res3*106
2Bh	Res3*44	Res3*43	6Bh	Res3*108	Res3*107
2Ch	Res3*45	Res3*44	6Ch	Res3*109	Res3*108
2Dh	Res3*46	Res3*45	6Dh	Res3*110	Res3*109
2Eh	Res3*47	Res3*46	6Eh	Res3*111	Res3*110
2Fh	Res3*48	Res3*47	6Fh	Res3*112	Res3*111
30h	Res3*49	Res3*48	70h	Res3*113	Res3*112
31h	Res3*50	Res3*49	71h	Res3*114	Res3*113
32h	Res3*51	Res3*50	72h	Res3*115	Res3*114
33h	Res3*52	Res3*51	73h	Res3*116	Res3*115
34h	Res3*53	Res3*52	74h	Res3*117	Res3*116
35h	Res3*54	Res3*53	75h	Res3*118	Res3*117
36h	Res3*55	Res3*54	76h	Res3*119	Res3*118
37h	Res3*56	Res3*55	77h	Res3*120	Res3*119
38h	Res3*57	Res3*56	78h	Res3*121	Res3*120
39h	Res3*58	Res3*57	79h	Res3*122	Res3*121
3Ah	Res3*59	Res3*58	7Ah	Res3*123	Res3*122
3Bh	Res3*60	Res3*59	7Bh	Res3*124	Res3*123
3Ch	Res3*61	Res3*60	7Ch	Res3*125	Res3*124
3Dh	Res3*62	Res3*61	7Dh	Res3*126	Res3*125
3Eh	Res3*63	Res3*62	7Eh	Res3*127	Res3*126
3Fh	**Res3*64**	Res3*63	7Fh	Res3*128	Res3*127

Res3 = V_{AVDD} / 128

GAMMA 1~14 output voltage — 0Ch~27h

Address	Name	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	GAMMA1	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA1[9:8]	
0Dh	GAMMA1	00h	GMA1[7:0]							
0Eh	GAMMA2	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA2[9:8]	
0Fh	GAMMA2	00h	GMA2[7:0]							
……	……	……	……	……	……	……	……	……	……	
……	……	……	……							
……	……	……	……	……	……	……	……	……	……	
……	……	……	……							
24h	GAMMA13	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA13[9:8]	
25h	GAMMA13	00h	GMA13[7:0]							
26h	GAMMA14	02h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GMA14[9:8]	
27h	GAMMA14	00h	GMA14[7:0]							

VGAMMA1~14 voltage formula

$V_{GAMMA1~14}$ = Res4 x $V_{GAMMA1~14}$_CODE

Res4 = V_{AVDD} / 1024

GAMMA1~14 output voltage (Unit: V)

DAC value	GAMMA1~14	DAC value	GAMMA1~14
0000h	0	0200h	Res4 *512
0001h	Res4 *1	0201h	Res4 *513
0002h	Res4 *2	0202h	Res4 *514
0003h	Res4 *3	0203h	Res4 *515
0004h	Res4 *4	0204h	Res4 *516
0005h	Res4 *5	0205h	Res4 *517
0006h	Res4 *6	0206h	Res4 *518
0007h	Res4 *7	0207h	Res4 *519
0008h	Res4 *8	0208h	Res4 *520
0009h	Res4 *9	0209h	Res4 *521
000Ah	Res4 *10	020Ah	Res4 *522
000Bh	Res4 *11	020Bh	Res4 *523
000Ch	Res4 *12	020Ch	Res4 *524
000Dh	Res4 *13	020Dh	Res4 *525
000Eh	Res4 *14	020Eh	Res4 *526
000Fh	Res4 *15	020Fh	Res4 *527
……	……	……	……
……	……	……	……
01F0h	Res4 *496	03F0h	Res4 *1008
01F1h	Res4 *497	03F1h	Res4 *1009
01F2h	Res4 *498	03F2h	Res4 *1010
01F3h	Res4 *499	03F3h	Res4 *1011
01F4h	Res4 *500	03F4h	Res4 *1012
01F5h	Res4 *501	03F5h	Res4 *1013
01F6h	Res4 *502	03F6h	Res4 *1014
01F7h	Res4 *503	03F7h	Res4 *1015
01F8h	Res4 *504	03F8h	Res4 *1016
01F9h	Res4 *505	03F9h	Res4 *1017
01FAh	Res4 *506	03FAh	Res4 *1018
01FBh	Res4 *507	03FBh	Res4 *1019
01FCh	Res4 *508	03FCh	Res4 *1020
01FDh	Res4 *509	03FDh	Res4 *1021
01FEh	Res4 *510	03FEh	Res4 *1022
01FFh	Res4 *511	03FFh	Res4 *1023

Channel Enable Register (with factory value) — 28h, (7Fh)

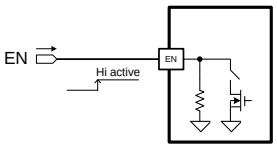
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Group B_EN	VGL_EN	VSS1_EN	AVDD_EN	HAVDD_EN	GMA_EN	VCOM1_EN	VGH_EN
0	1	1	1	1	1	1	1

Group B: AVDD, HAVDD, VGH, VGL, VSS1, Gamma, VCOM1, VCOM2DAC, L/S output.
0: Channel disable
1: Channel enable

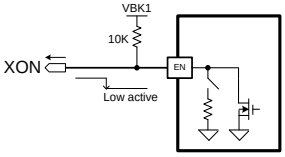
Delay Power Off and XON Register (with factory value) — 31h, (02h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EN_PIN_SEL	VCOM1_DLY_OFF	HAVDD_DLY_OFF	GMA_DLY-OFF	XON_DIS_THR	XON_DIS_THR	XON_DIS_THR	XON_DIS_THR
0	0	0	0	0	0	1	0

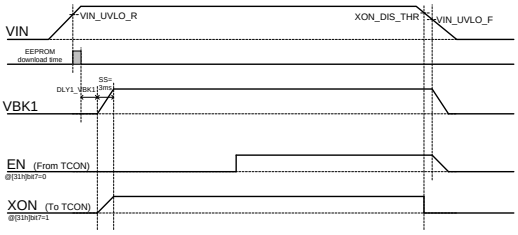
Bit	Name	Description
Bit7	EN_PIN_SEL	EN pin function select 0: Enable pin of the AVDD, VGH, HAVDD, VCOM and Gamma. Enable pin must be connect high signal. 400kohm pull down resistor connect from this pin to ground. 1: XON pin for the shutdown reset function output and open drain voltage detector output.



Bit7=0, EN function

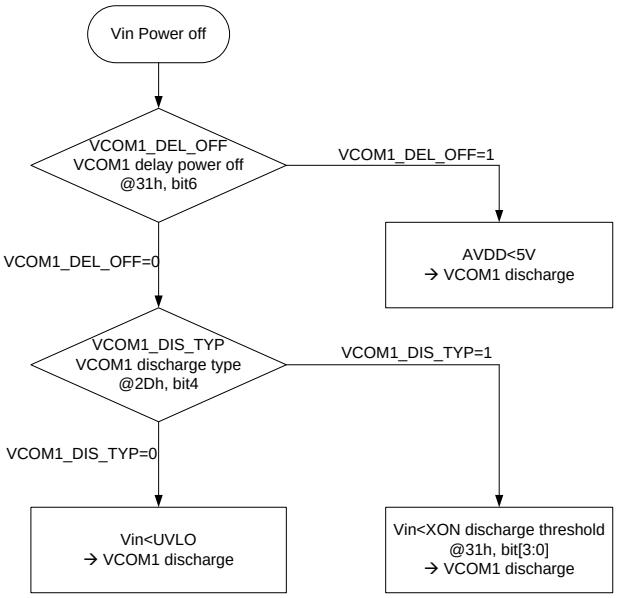


Bit7=1, XON function



EN and XON function of power sequence

Bit	Name	Description
Bit6	VCOM1_DLY_OFF	VCOM1 delay power off 0: Disable 1: Enable



VCOM2DAC (with factory value) — 45h, (7Eh)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	1	1	1	1	1	Reserved

VCOM2DAC_NT voltage formula
VCOM2DAC=Res1*VCOM2DAC CODE +VCOM_MIN
Res1=(VCOM_MAX-VCOM_MIN)/127
VCOM2DAC CODE= 0 ~ 127

VCOM2DAC Enable Register (with factory value) — 46h, (00h)
Monitor Mode Enable Register — 46h, (00h)

Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
MNT_MODE_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCOM2DAC_EN

VCOM2DAC Enable
0: Channel disable
1: Channel enable

MNT MODE Enable
0 : TV MODE (VIN=12V)
1 : MNT MODE (VIN=5V)

Register Map
Device address (E8h/E9h)

Address	Name	Description	Default value	Reso-lution	Range
00h	RESET	[4] Down load VCOM1_NT data from EEPROM to DAC register	0: Disable		0: Disable 1:Enable
	VCOM1_NT_WR_EPM	[3] Write VCOM1_NT data from DAC register to EEPROM.	0: Disable		0: Disable 1:Enable
	OUT_EN	[1] VCOM1 output enable	1: Enable		0: Disable (VCOM1 output Hi-z) 1: Enable
01h	VCOM1_NT	[7:1] VCOM1_NT normal temper-ature voltage	63*Res1+VCOMMIN (7Eh)	Res1	VCOM_MIN(0Dh) to VCOM_MAX(0Eh) Res1=(VCOM_MAX-VCOM_MIN)/127
02h	FAULT FLAG	[7] OTP	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[6] Level Shift NG	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[5] VBK1 UVP or SCP	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[4] AVDD UVP or SCP	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[3] VGH UVP or SCP	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[2] VGL UVP or SCP	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[1] VSS1 UVP	0: Disable		0: Disable 1:Enable Read only, Release IC restart
02h	FAULT FLAG	[0] HAVDD UVP or SCP	0: Disable		0: Disable 1:Enable Read only, Release IC restart

VCOM1 control (with factory value) — 00h, (02h)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Reserved	RESET	WR to NVM	Reserved	OUT_EN	Reserved

Bit	Name	Description
Bit4	RESET	Down load VCOM1_NT data from EEPROM to DAC register 0: disable 1:enable
Bit3	WR to NVM	Write VCOM1_NT DAC data from DAC register to EEPROM 0: disable 1:enable
Bit1	OUT_EN	VCOM1_NT DAC output enable 0: disable (VCOM1 output is Hi-Z) 1:enable

VCOM1_NT (with factory value) — 01h, (7Eh)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	1	1	1	1	1	1	Reserved

VCOM1_NT voltage formula

VCOM1_NT=Res1*VCOM1_NT CODE +VCOM_MIN
Res1=(VCOM_MAX-VCOM_MIN)/127
VCOM_NT CODE= 0 ~ 127

Protection Table

Group A: VBK1

Group B: AVDD, HAVDD, VGH, VGL, VSS1/2, Gamma, VCOM1, VCOM2DAC, L/S output

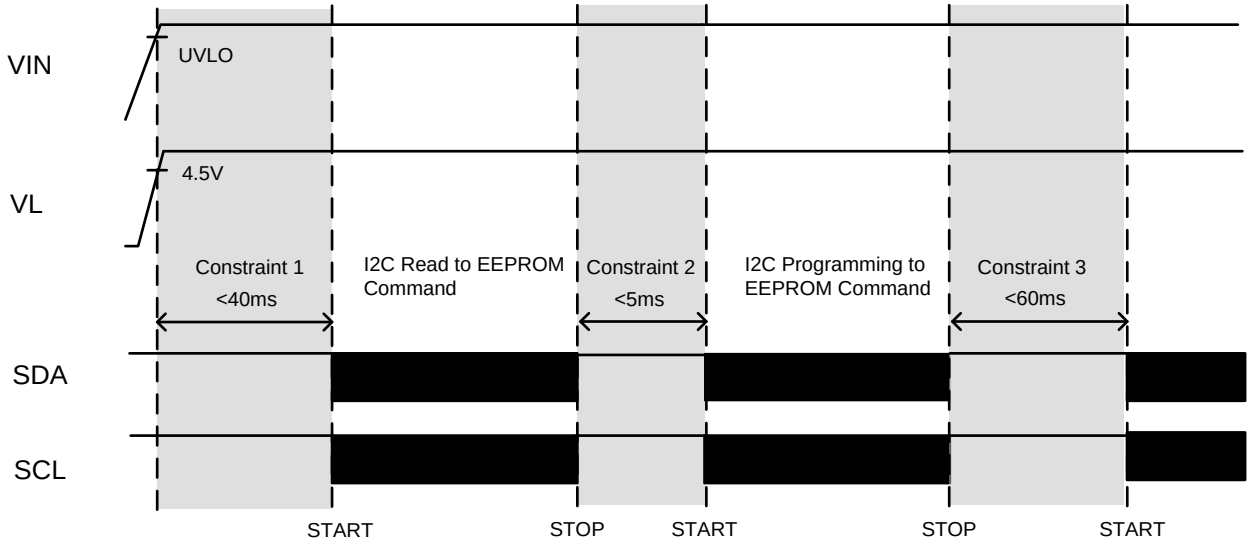
	Protection Function	Work Condition	Action	Remark
VBK1	OCP	1.5A	--	--
	UVP	VBK1 < 80%, after 50ms	IC Group A / B shut down, latch	Release IC restart
	SCP	VBK1 < 20%	IC Group A / B shut down, latch	Release IC restart
	OVP	VBK1 >120%	LXBK1 stop switching	Release OVP-hysteresis
AVDD	OCP	5.0A	--	--
	UVP	AVDD < 85%, after 50ms	IC Group B shut down, latch	Release IC restart
	SCP	AVDD < 20%	IC Group B shut down, latch	Release IC restart
	OVP	AVDD >21.8V	LX/CS stop switching	Release OVP-hysteresis
HAVDD	OCP	+/-200mA Typ.	--	--
	UVP	HAVDD < 80%, after 50ms	IC Group B shut down, latch	Release IC restart
	SCP	HAVDD <20%	IC Group B shut down, latch	Release IC restart
	OVP	HAVDD>120%, after 50ms	IC Group B shut down, latch	Release IC restart
VGH	OCP	1.5A	--	Boost mode only
	UVP	VGH < 80%, after 50ms	IC Group B shut down, latch	Release IC restart
	SCP	VGH < 20%	IC Group B shut down, latch	Release IC restart
	OVP	VGH>48.5V	LXVGH stop switching	Release OVP-hysteresis
VGL	OCP	1.5A	--	Inverting mode only
	UVP	VGL < 80%, after 50ms	IC Group B shut down, latch	Release IC restart
	SCP	VGL <20%	IC Group B shut down, latch	Release IC restart
	OVP	VGL >120%	LXVGL stop switching	Release OVP-hysteresis
VSS1	OCP	+/-100mA Typ.	--	--
	UVP	VSS1 < 80%, after 50ms	IC Group B shut down, latch	Release IC restart
GAMMA	Current limit	+/-180mA Typ.	--	--
VCOM1	Current limit	+/-400mA Typ.	--	--
PMIC	OTP	IC Tj>150℃ Typ.	IC Group A/B shut down, latch	Release IC restart

Note : SCP and OVP is trigger immediate, no trigger time.

Layout Considerations

- Power loops of the converters should be connected with the shortest and widest traces as possible. The long and narrow trace increases the ESR and ESL, and that will induce more effective noise at high frequency easily.
- The placements of the input bypass capacitor must be as close as possible to the G2732P to reduce the input ripple voltage and noise coupling. The ground of input bypass capacitor must connect near to the IC's ground pin.
- The compensation network should connect to G2732P as close as possible. Each output voltage feedback route should keep away from any switching node.
- The Exposed Pad should be connected to a strong ground plane for maximum thermal consideration.

I²C Communication Timing Chart



Constraint 1: EEPROM start up blanking time.

It is the time from AVIN/VL powered up (after UVLO threshold) to the end of loading EEPROM data to DAC. Any attempt from the I²C master talking to G2732P is not acknowledged.

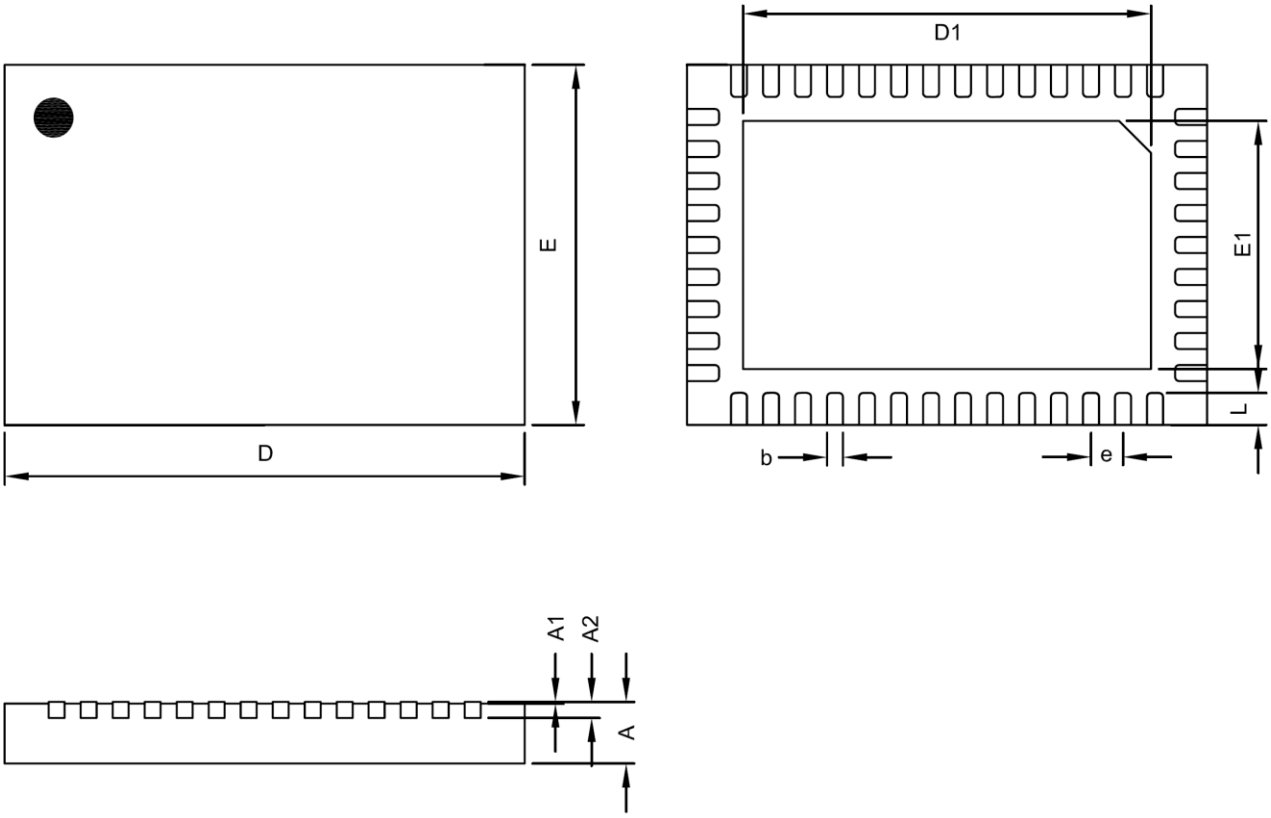
Constraint 2: Read to EEPROM blanking time

It is the time from a valid stop condition of a EEPROM read command to the end of the internal operation cycle. Any attempt from the I²C master talking to G2732P is not acknowledged.

Constraint 3: Programming EEPROM blanking time.

It is the time from a valid stop condition of a EEPROM write command to the end of internal EEPROM programming operation. Any attempt from the I²C master talking to G2732P is not acknowledged.

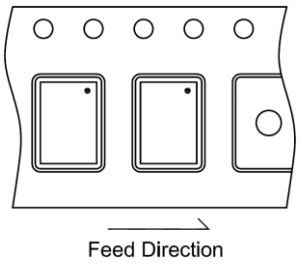
Package Information



TQFN6.5X4.5-46 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	6.45	6.50	6.55	0.2539	0.2559	0.2579
E	4.45	4.50	4.55	0.1752	0.1772	0.1791
D1	5.00	5.10	5.20	0.1969	0.2008	0.2047
E1	3.00	3.10	3.20	0.1181	0.1220	0.1260
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN6.5X4.5-46	3,000 ea

GMT Inc. does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and GMT Inc. reserves the right at any time without notice to change said circuitry and specifications.

Revision History

Version	Contents
20211028	New Release
20211101	1. Order number G2732PK81D 改為 "G2732PK81D-K" 2. Page 12 說明修正紅字部分: AVDD external mode, VGH boost type, VGL inverting type HAVDD Internal FB, VCOM2 Enable 3. Page 12 圖檔修正 Buck 1 為同步線路 4. Page 13 說明修正紅字部分: AVDD internal mode, VGH charge pump type and VGL charge pump type HAVDD External FB, VCOM2 Disable 5. Page 5 Load Regulation: I_{GL} = 200mA to 500mA ->TYP=0.3%/A 6. Page 13 電路圖加註描述: * VGL Charge pump type use LXBK1 only for TV Mode [@[46h] bit7=0]